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Fault-Tolerant Galvanically Isolated DC-DC Converters with Zero Redundancy

Abualkasim Ahmed Ali Bakeer

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

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ABUALKASIM AHMED ALI BAKEER

Contents

List of Publications

A list of the author's publications, based on which the thesis has been prepared:

[PAPER-I] **A. Bakeer**, A. Chub, and D. Vinnikov, "Full-Bridge Fault-Tolerant Isolated DC-DC Converters: Overview of Technologies and Application Challenges," in IEEE Power Electronics Magazine, vol. 9, no. 3, pp. 45–55, Sept. 2022, doi: 10.1109/MPEL.2022.3196565.

[PAPER-II] **A. Bakeer**, A. Chub, and D. Vinnikov, "Study of MOSFET Post-Fault Operation in Fault-Tolerant DC-DC Converters," in proc. IEEE 7th International Energy Conference (ENERGYCON), 2022, pp. 1–5, doi: 10.1109/ENERGYCON53164.2022.9830216.

[PAPER-III] **A. Bakeer**, A. Chub, and D. Vinnikov, "Short-Circuit Fault Detection and Remedial in Full-Bridge Rectifier of Series Resonant DC-DC Converter Based on Inductor Voltage Signature," in proc. IEEE 61st International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), 2020, pp. 1–6, doi: 10.1109/RTUCON51174.2020.9316482.

[PAPER-IV] **A. Bakeer**, A. Chub, A. Blinov, and J.-S. Lai, "Wide Range Series Resonant DC-DC Converter with a Reduced Component Count and Capacitor Voltage Stress for Distributed Generation," in Energies, vol. 14, no. 8, MDPI AG, p. 2051, Apr. 07, 2021. doi: 10.3390/en14082051.

[PAPER-V] **A. Bakeer**, A. Chub, D. Vinnikov, and F. Blaabjerg, "Effect of Mission Profile Resolution on Photovoltaic Energy Yield Prediction in Python and MATLAB," in proc. IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), 2021, pp. 1–5, doi: 10.1109/CPE-POWERENG50821.2021.9501222.

[PAPER-VI] **A. Bakeer**, A. Chub, and Y. Shen, "Reliability Evaluation of Isolated Buck-Boost DC-DC Series Resonant Converter," in IEEE Open Journal of Power Electronics, vol. 3, pp. 131–141, 2022, doi: 10.1109/OJPEL.2022.3157200.

[PAPER-VII] **A. Bakeer**, A. Chub, and D. Vinnikov, "Self-Healing Photovoltaic Microconverter with Zero Redundancy and Accurate Low-Cost Fault Detection," in IEEE Transactions on Industrial Electronics, accepted for publication, 2023, doi: 10.1109/TIE.2023.3250836.

Author's Contribution to the Publications

Contribution to the papers in this thesis are:

[PAPER-I] Abualkasim Bakeer, as the primary author, was responsible for the methodology and preparing the survey of topologies. He also developed the reliability part associated with the faulty state of the converter with and without the power curtailment. He wrote the first draft and prepared the response to the editor and reviewers during the peer-review process.

[PAPER-II] Abualkasim Bakeer, as the primary author, was responsible for the methodology, software, and experimental validation. He wrote the paper's first draft and drew all the paper's figures. He was responsible for submitting and contacting the conference during the publication step. He prepared the PowerPoint presentation and presented the article physically at the Latvian conference in May 2022.

[PAPER-III] Abualkasim Bakeer, as the primary author, was responsible for the methodology, software, and simulation validation. He wrote the first draft of the paper. He was responsible for submission and contacting the conference during the publication step. He prepared the PowerPoint presentation and presented the paper online at the virtual conference event in Latvia.

[PAPER-IV] Abualkasim Bakeer, as the primary author, was responsible for the main idea, methodology, software, and experimental validation. He wrote the first draft of the paper. He was also responsible for preparing the response to the editor and reviewers during the peer-review process.

[PAPER-V] Abualkasim Bakeer, as the primary author, has developed the methodology of the paper and prepared the required software based on Python and MATLAB. In addition, he wrote the first draft and prepared the presentation for the conference.

[PAPER-VI] Abualkasim Bakeer, as the primary author, was responsible for the main idea, methodology, software, and experimental validation. He wrote the first draft of the paper and drew all the figures. He was responsible for submission and contacting the journal during the publication step. He was also responsible for preparing the response to the editor and reviewers during the peer-review process.

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Abbreviations

AC	Alternating current
APWM	Asymmetric pulse width modulation
DC	Direct current
FFT	Fourier fast transform
FHR	Forced half resonance
FT	Fault-tolerant
GND	Ground
IB	Input bridge
IBBC	Isolated buck-boost converter
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-gate bipolar transistor
LLC	Inductor-Inductor-Capacitor resonant converter
MG	Microgrid
MIL-HDBK-217F	Military Handbook: Reliability Prediction of Electronic Equipment
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPP	Maximum power point
MPPT	Maximum power point tracking
MTTF	Mean time to failure
OB	Output bridge
OCF	Open-circuit fault
P&O	Perturb and observe
PCB	Printed circuit board
PSM	Phase-shift modulation
PV	Photovoltaic
PWM	Pulse width modulation
RESs	Renewable energy sources
SRC	Series resonant converter
SCF	Short-circuit fault
Si	Silicon
SiC	Silicon carbide
TMC	Topology morphing control
UPS	Uninterrupted power supply
VDR	Voltage doubler rectifier
ZR	Zero-redundancy
ZVS	Zero voltage switching

Symbols

I_{PV}	PV current (A)
V_{PV}	PV voltage (V)
V_{in}	Input voltage (V)
I_{Lr}	Resonant inductor current (A)
Z_r	Resonant impedance (Ω)
F_{sw}	Switching frequency (Hz)
T_{sw}	Switching period (s)
F_r	Resonant frequency (Hz)
P_{out}	Output power (W)
n	Transformer turns ratio
Q	Quality factor
R	Load resistance (Ω)
L_r	Resonant inductance (H)
C_r	Resonant capacitance (F)
C_b	Blocking capacitance (F)
C_{in}	Input capacitance (F)
C_o	Output capacitance (F)
V_p	Voltage of the primary winding of the transformer (V)
V_s	Voltage of the secondary winding of the transformer (V)
V_1	Output voltage of the inverter bridge (V)
V_2	Input voltage of the rectifier bridge (V)
i_m	Magnetizing current (A)
v_{Cr}	Resonant capacitor voltage (V)
v_{Cb}	Blocking capacitor voltage (V)
V_{Q2}	Drain-source voltage of the switch Q_2 (V)
V_{Q4}	Drain-source voltage of the switch Q_4 (V)
$V_{gs,Q1}$	Gate-source voltage of the switch Q_1 (V)
$V_{gs,Q2}$	Gate-source voltage of the switch Q_2 (V)
$R_{ds,on}$	MOSFET drain-source resistance (Ω)
λ	Item random failure rate (failure/10^6 hours)
λ_b	Basic failure rate
π_T	Temperature stress
π_A	Application stress
π_Q	Quality stress
π_E	Environmental stress
π_C	Capacitance stress
π_V	Voltage stress
Π_{PM}	Technical and quality during manufacturing of the item
$\Pi_{Process}$	Stages of the item processes
λ_{Phy}	The physical failure rate of the item

N	Number of converter components
R_n	Reliability of an item
λ_{IBBC}	IBBC failure rate
$V_{IN,Nom}$	Nominal input voltage (V)
V_{MG}	DC microgrid voltage
B	Peak-to-peak flux density in the core (Wb/m^2)
N_p	Primary turns
A_c	The effective cross-section area of the core (cm^2)
$V_{IN,min}$	Minimum input voltage (V)
$I_{IN,max}$	Maximum input current (A)
ω_r	Resonant angular frequency (rad/s)
C_{oss}	Parasitic output capacitance (F)
T_{DT}	Dead-time (s)
ΔV_{Cr}	Peak-to-peak voltage ripple across the resonant capacitor (V)
V_{MPP}	PV voltage at maximum power point (V)

1 Introduction

1.1 Background

The leading cause of climate change in the world is the significant greenhouse gas emissions from human activities. In recent years, state and regional governments have proposed many incentives to curb climate change. With climate change becoming increasingly evident worldwide, electrification is considered a viable solution for the energy transition. Furthermore, the electrification of commonplace systems in industrial and residential sectors is expected to increase rapidly. One of the renewable energy sources is photovoltaic (PV) energy, which is considered environmentally friendly. Its use has increased significantly due to modern technologies that lead to lower prices. However, there are challenges associated with operating residential PV systems under partial shade conditions due to the accumulation of snow or leaves, shading from trees or rooftop structures, and partial shade from neighboring trees. Partial or opaque shading conditions could result in the wide variation of a photovoltaic module's global maximum power point voltage during the day and intermittent variations in daily solar irradiance. In addition, the PV module's input voltage decreases with shadow due to varying surrounding conditions.

With critical applications such as medical devices, aircrafts, and data centers, the conception of the reliability of the power converters has a high priority level when selecting the power converter from among the available ones on the global market [1]. In these cases, the power converter should provide continuity to feed the different services with existing faults despite the low performance, such as a high voltage/current ripple and low efficiency. Therefore, using fault-tolerant (FT) DC-DC converters in mission-critical applications is increasingly popular in order to defer after-fault maintenance [2]. Thus, the architecture of the interface DC-DC converter must have the following characteristics: the ability to control the input voltage in a wide range, galvanic isolation, high power density, and reliability so that high efficiency is ensured [3].

The isolated flyback and forward converters are usually employed for low-power applications. Despite these topologies being simple and cost-effective, they do not allow post-fault operation and can not regulate the wide range of input voltage variations. One possible way to overcome this is by adding (N+1) conventional redundancy, increasing the implementation and maintenance costs [PAPER-I]. The series resonant converter (SRC) is a promising isolated DC-DC converter topology that could regulate the wide input voltage variation with voltage buck or boost capability. In addition, it has the feature of direct power transfer into the load during most of the switching period. The basic concept of FT zero-redundancy SRC (ZR-SRC) is based on topology reconfiguration, allowing the converter to continue operating after a fault without adding more components.

1.2 The Motivation of the Thesis

Power electronics converters are considered the most vulnerable to failure in the power conversion systems for renewable energy sources (RESs) compared to the other components. According to industrial statistics, power semiconductors represent approximately 31% of power electronic converter failures [4], as shown in Figure 1.1. Fault-tolerant implementation approaches can help to improve the reliability of power electronics converters. These approaches ensure the system remains operational even if a few components fail. A power electronics converter for PV module-level applications is usually rated to operate for at least 25 years. This duration corresponds to the expected lifetime of a PV module. A converter could employ fault tolerance to increase its lifetime towards this goal. The primary attention should be on the semiconductors fault, particularly the open- and short-circuit faults.

The research work in this thesis was conducted according to one of the research directions of the Power Electronics Group of Tallinn University of Technology. This thesis gathers knowledge and develops fault-tolerant zero-redundancy implementation techniques and corresponding fault diagnosis and detection methods for an SRC-based microconverter aimed at residential PV applications connected to the DC microgrid (MG). As a result, it should achieve minimum redundancy and, consequently, low implementation cost acceptable in residential applications. The Estonian Research Council supported the current work under the grant of PSG206 “DC-DC Converters with Ultra-Wide Regulation Range and Post-Fault Operation Capability” and PRG1086 “Future-Proof Power Electronic Systems for Residential Microgrids.”

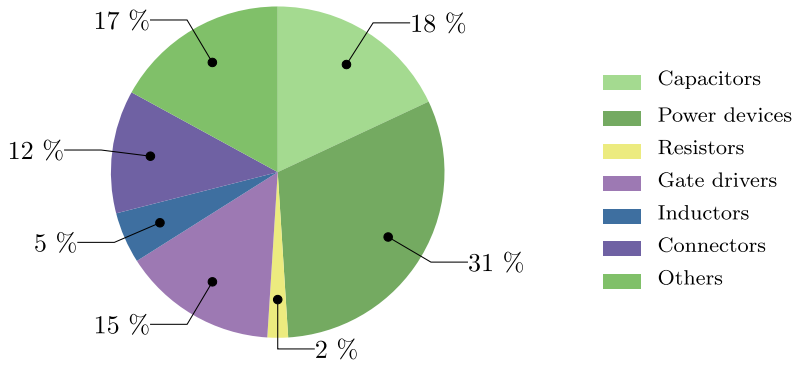


Figure 1.1 Distribution of faults in power electronics converter’s components.

1.3 Aims, Hypotheses, and Research Tasks

The main aim of the Ph.D. research project is to develop and experimentally confirm the concept of fault-tolerant zero-redundancy galvanically isolated DC-DC converters with a wide input voltage range and post-fault operation capability for interfacing PV modules into the residential DC microgrid. The proposed solution enables post-fault operation using low-cost techniques. As a result, a new generation of residential DC-coupled PV systems could be designed to provide satisfactory performance over the lifetime expectancy of the PV module. Furthermore, residential photovoltaic applications will be more affordable due to the lower lifecycle costs of the technology used.

Hypotheses:

1. The fault tolerance could be achieved in a galvanically isolated buck-boost DC-DC converter with zero redundant components.
2. Post-fault operation of DC-DC converters with reconfigurable switching cells could be achieved by utilizing the short-circuited switch as a current conducting path.
3. Taking into account the influence of the application-specific mission profile on the random failure rate of the converter's components would allow the possibility for application-tailored design and estimation of pre- and post-fault converter lifetime.
4. Applying an FT converter with input power curtailment in the PV applications would allow maintaining the same converter failure rate after the faulty state while reducing the annual energy yield by no more than 20%.

Research tasks:

1. To review the FT isolated converters based on the SRC, showing the pros and cons of each.
2. To investigate the feasibility of using the faulty switch as a current conduction path in the case of a short-circuit fault.
3. To compare the fault detection and diagnosis methods in terms of the complexity and cost of the implementation.
4. To synthesize the random failure rate estimation method for DC-DC converters, considering application-specific mission profiles.
5. To develop accurate and fast fault detection methods capable of localizing a faulty semiconductor component.
6. To develop a low-cost interface converter for residential PV modules that can maintain the failure rate as normal after the semiconductor's fault.

1.4 Research Methods

The research methods used in the thesis are based on mathematical analysis of electronic circuits in the time domain using volt-second and ampere-second balance, numerical simulation models in PLECS and PSIM software, and experimental prototype verification. The converter loss model is built in the PLECS software using the datasheet parameters of the component used in the prototype. This allows us to synthesize thermal models that could be further used to investigate the reliability of the studied isolated buck-boost converter (IBBC) under the yearly mission profile of solar irradiation and ambient temperature. Computer simulations are generally performed in Python, MATLAB, PLECS, and PSIM software packages, most of which are available at the Tallinn University of Technology (TalTech). Altium Designer was used for the design of electric circuits and PCB development. Cloud software evaluating the reliability of the IBBC was developed in Python to achieve high execution speed resulting from using scientific and numerical libraries based primarily on optimized C-code. Finally, the experimental assessment was performed using laboratory prototypes of the studied converters to corroborate the theoretical predictions. The Power Electronics Research Laboratory of TalTech provides cutting-edge facilities for numerical simulations, hardware prototyping, and firmware development: laboratory DC power supplies, programmable DC electronic loads, solar array simulators, digital oscilloscopes, and corresponding probes with a wide bandwidth (>100 MHz), precision power analyzer, microprocessor development tools, PCB prototyping, soldering tools, and all other essential equipment.

1.5 Contributions and Disseminations

The research results are presented through scientific publications, conferences, symposiums, doctoral schools, and presentations. During his Ph.D. studies, the author contributed to seven publications. Among them, four articles have been published in peer-reviewed journals of the IEEE. The conference papers were reported at international events after undergoing a peer-review process. This thesis is written based on seven scientific publications, including four journal and three conference papers.

Scientific novelties:

- Development, justification, and demonstration of the zero-redundancy fault tolerance concept in galvanically isolated DC-DC converters.
- The methodology for predicting the lifetime of the DC-DC converters, which is taking into account the influence of the application-specific mission profile on the random failure rate of components.
- The fault detection method for PV microconverters reusing the existing current and voltage sensors, which can provide fast, low-cost, and accurate localization of a faulty semiconductor device.
- Applications of the PV power curtailments technique to the fault-tolerant zero-redundancy DC-DC converters to maintain the same failure rate in post-fault conditions and methodology of its design.

Practical novelties:

- Experimental analysis of post-fault resistance of low-voltage Si and high-voltage SiC MOSFETs.
- Design of the PV microconverter with zero redundancy for residential applications with fault-tolerant capability.
- Demonstration of the lifetime underestimation for the PV microconverters resulting from using the MIL-HDBK-217F handbook.
- Recommendations for designing PV power curtailment algorithm for the case of post-fault operation of the FT zero-redundancy PV microconverter with 60-cell Si PV module.
- Measuring and providing an open-source yearly mission profile of solar irradiance and ambient temperature for Tallinn, Estonia.

1.6 Experimental Setup and Equipment

The experimental setup was assembled in the power electronics laboratory of Tallinn University of Technology. The tested prototype is shown in Figure 1.2. The waveforms of voltages and currents have been captured with the Tektronix MDO4034B-3 oscilloscope. Voltage and current waveforms were measured using differential voltage probes Tektronix P5205A and current probes TCP0030A, respectively. The firmware for STM32 microcontrollers was developed in the Keil µVision integrated development environment. Precision power analyzer Yokogawa WT1800 was employed to measure converter efficiency using the software application WTViewer for remote equipment access. The Agilent E4360 series modular solar array simulator was used as an input power

source for the experimental prototype while testing under the daily mission profiles. The Chroma 63205A-600-350 DC electronic load was employed to emulate the DC microgrid at the output of the IBBC.

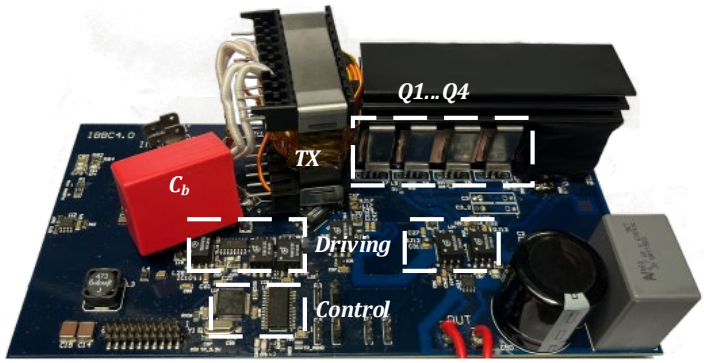


Figure 1.2 Prototype of the fault-tolerant PV microconverter.

1.7 Recording of the Solar Mission Profile in Tallinn

The mission profile of solar irradiance and ambient temperature was recorded in Tallinn, Estonia, to share openly with the research community. The complete setup is installed on the rooftop of the NRG building, Tallinn University of Technology. A low-cost solution based on the Arduino platform is used as the main component for the data logger. The total installed system is shown in Figure 1.3. The DS1307 serial real-time lock is utilized to record real-time measurements. The solar irradiance is measured using three small PV cells connected in parallel to increase the total current. Following this, the short-circuit current is measured by the ACS70331 current sensor, which has a range of 2.5 A. A low-cost digital temperature sensor DS18B20 was used to measure the ambient temperatures with up to 12-bit resolution in centigrade. It can transfer readings to a microprocessor using a 1-Wire bus that only needs one data line for communication and two more for power supply and ground (GND) signals. It has an accuracy of ±0.5 ^{o}C when the temperature is between -10 ^{o}C and +85 ^{o}C. It has been installed in the shade outside the main box. The data are stored in an SD card using the SD card shield for Arduino [5].

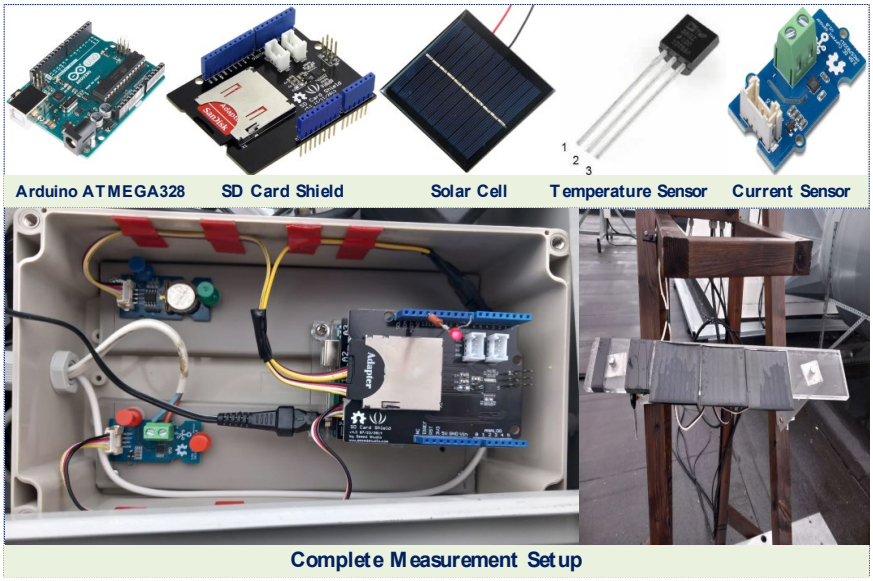


Figure 1.3 Weather station recording solar irradiance and ambient temperature – installed on the roof of NRG building, Tallinn University of Technology, Tallinn, Estonia.

1.8 Thesis Outline

The remaining part of the thesis starts with Chapter 2, which discusses the state-of-the-art isolated FT topologies based on the SRC. Following this, Chapter 3 explains the proposed isolated FT ZR-SRC and the fault detection issues. Chapter 4 introduces the proposed methodology for evaluating the IBBC reliability under a yearly PV mission profile based on the FIDES Guide. The modulation technique and the design guidelines are given in Chapter 5 based on the proposed methodology to diagnose and identify the IBBC fault on the input/output sides. Finally, Chapter 6 concludes the thesis and provides future work directions.

2 Literature Review

2.1 Introduction

It is typical for high step-up DC-DC applications to require galvanic isolation to step up the voltage efficiently. Therefore, several DC-DC converters have been proposed to address voltage variation [1],[6]. Various topologies provide different complexity, efficiency, implementation cost, and other aspects. Isolated buck-boost converters are suitable for wide-range applications requiring high voltage step-up. Usually, they have active switches on both sides of the converter to implement voltage buck and boost functionalities. Among these topologies, series resonant converters (SRCs) have demonstrated high performance in the target PV applications. The SRC topology provides soft-switching of semiconductor components, good isolation transformer utilization, and similarity to the LLC converter topology investigated in many industrial applications [7]. However, the ratio between the magnetizing and the resonant inductances is several times higher in the SRC than in the LLC converter.

The resonant frequency (F_r) of the resonant converters can be given as in (2.1), where L_r is the resonant inductance, and C_r is the resonant capacitance. Resonant converters primarily depend on the quality factor (Q) that is affected by the parameters of the resonant tank and the load value (R) as in (2.2). The quality factor refers to the peak stored energy in the circuit to dissipate energy into the load.

Figure 2.1 describes the relationship between the quality factor and the circuit parameters, where F_{SW} is the switching frequency. Notably, the DC voltage conversion gain of the converter can be controlled by changing the switching frequency, i.e., frequency modulation. However, this design results in low voltage regulation performance at light loads, making the design of magnetic components more challenging. Therefore, operating SRC at fixed switched efficiency is more efficient.

$$F_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.1}$$

$$Q = \frac{1}{R}\sqrt{\frac{L_r}{C_r}} \tag{2.2}$$

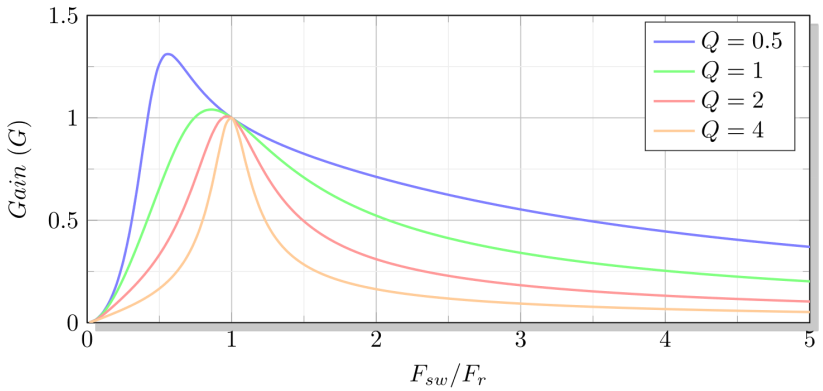


Figure 2.1 Conversion gain of SRC with frequency modulation at different quality factor (Q) values.

2.2 Classifications of SRC Fault-Tolerant Topologies

This subchapter discusses three possible implementations of fault-tolerant galvanically isolated full-bridge DC-DC converters and their pros and cons based on [PAPER-I]. The main concern of SRC failure is semiconductor failure. For these converters, the reported statistics show that primary semiconductors are the most vulnerable components [8].

Converter semiconductors generally have two possible fault states depending on the failure mechanism: open-circuit fault (OCF) and short-circuit fault (SCF). There are three main approaches to achieving fault tolerance in full-bridge galvanically isolated DC-DC converters for semiconductor faults, as summarised in Table 2.1. Using redundant components to overcome converter failure conditions is considered the most common and straightforward way to prevent power outages in mission-critical applications such as data centers and smart transformers [14], [15]. This allows the converter to extend its useful lifetime and increase its availability. The mentioned redundancy refers to the component level within a single converter. This requires additional hardware in the converter design, such as semiconductor or electromechanical switches, capacitors, bypass switches, and fuses, to isolate the defective component.

Table 2.1 Comparison between implementation approaches of the DC-DC FT-SRC.

Item	**Redundant active leg [9]**	**Redundant capacitors leg [10],[11]**	**Zero redundancy [12], [13]**
Example	Figure 2.2	Figure 2.3	Figure 2.4
IB/OB switch type	IGBT	MOSFET/IGBT	MOSFET/IGBT
Reported power range	> 350 W	> 350 W	< 350 W
Post-fault overloading of components	No	Yes	Yes
Power curtailment	Not Needed	Needed	Needed
Additional components	• 4 Aux. switches • 4 Semiconductors • 8 Fuses	• 4 Aux. switches • 0 Semiconductors • 0 Fuses	• 0 Aux. switches • 0 Semiconductors • 0 Fuses
Power density	XXX	XX	X
Cost	$$$	$$	$
Reported applications	• Uninterruptable power supply • Data centers	• Uninterruptable power supply • Data centers	• Residential PV • Battery charger • Light-emitting diodes

- X is the smallest, XXX is the largest
- $ is the cheapest, $$$ is the most expensive

2.2.1 Topologies with Redundant Semiconductors

This FT implementation approach uses redundant switching legs (i.e., active legs) on the input and output sides. It requires a fuse in each semiconductor in the converter to convert the SCF to OCF after a thermal breakdown [9], as shown in Figure 2.2, in which V_{in} is the input voltage, V_o is the output voltage, i_m is the magnetizing current, i_{Lr} is the resonant inductor current, and v_{Cr} is the resonant capacitor voltage. By doing this, the short-circuited faulty switch is isolated. To completely isolate the faulty leg, the healthy switch of the faulty leg should be turned off continuously. However, one of the drawbacks of using the fuses is that they consume power as they are connected in series during normal operation and thus affect the converter efficiency [8]. In addition, the presence of the fuse will increase parasitic inductance in the circuit [9].

Moreover, the auxiliary leg in such an FT converter implies additional costs for the auxiliary switches, gate drives, and auxiliary power supply. On the other hand, with this FT implementation approach, the converter component can handle the same power before and after the fault occurrence without overloading, as they are generally designed in the same way as the main inverter legs. This FT implementation approach typically utilizes IGBTs that can handle the short-circuit current long enough to burn the fuse. This ruggedness is unavailable with generic MOSFETs essential in low-power applications. An IGBT can easily withstand a short-circuit current for 10 µs, while some detection methods require less than one switching period to detect the fault [16].

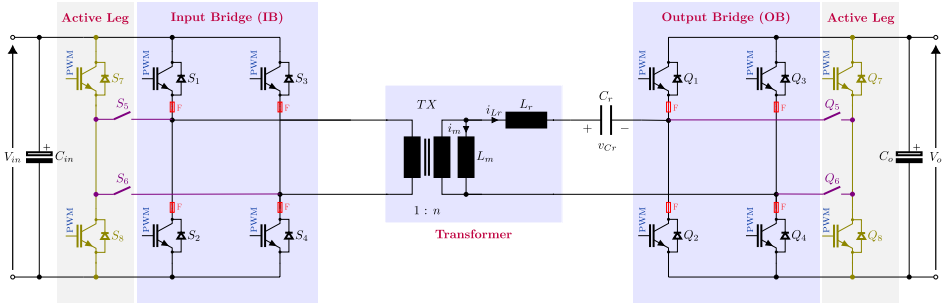


Figure 2.2 A fault-tolerant isolated DC-DC converter using redundant semiconductor components on the input and output sides.

2.2.2 Topologies with Redundant Capacitors

This FT implementation approach has two split capacitors with midpoints on the input and output sides, as shown in Figure 2.3 [10]-[11]. It requires four bypass switches to connect the faulty leg to these midpoints. Unlike the previous FT approach based on the active redundant leg, the IB/OB can be realized using IGBTs or MOSFETs, and the fuses are not required. The key to this FT approach is to keep the converter running after a failure but as a half-bridge SRC instead of a full-bridge SRC on the input side. In contrast, the output side will be reconfigured into a voltage doubler rectifier (VDR). The IB or OB should be reconfigured using the additional bypass switches to obtain an entire FT-SRC operation. In the case of an SCF, the damaged switch is used as a current conduction path, while another switch on the same leg is disconnected to prevent a short circuit across the power supply terminals. Since the power going to the load is the same before and after the fault, the converter on the opposite side will be over-stressed.

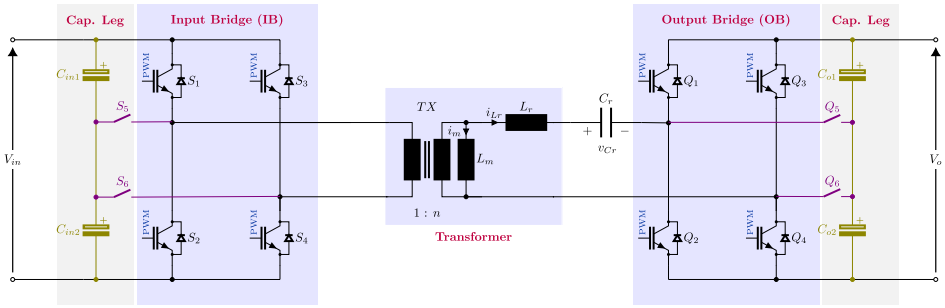


Figure 2.3 A fault-tolerant isolated DC-DC converter using redundant capacitors on the input and output sides.

2.2.3 Topologies with Zero Redundancy

The fault-tolerant zero-redundancy SRC (FT ZR-SRC) is shown in Figure 2.4 [12], where V_1 is the output voltage of the input inverter, V_2 is the input voltage of the output rectifier, Vp is the primary winding voltage, V_s is the secondary winding voltage, and V_{Cb} is the voltage across the blocking capacitor C_b. This converter features buck and boost operation modes using special modulation techniques for its IB and OB, respectively. This concept is an alternative realization of the bidirectional SRC to ensure the post-fault operation in the case of SCF or OCF in any of its semiconductors. This topology has unique FT capabilities. The proposed FT implementation approach can be referred to as topology reconfiguration, which provides self-sufficiency without adding additional components to the circuit. This concept has been applied industrially in the photovoltaic (PV) microconverter named Optiverter [13]. The FT ZR converter can withstand a single fault (OCF or SCF) of its IB/OB semiconductors with up to two semiconductor faults without adding additional components. This is achieved by reconfiguring the faulty bridge as a half-bridge if the other bridge has an SCF.

Similarly to the FT implementation with redundant capacitors, the output voltage of the FT-SRC remains constant after a fault, and the RMS current of the transformer and the semiconductor becomes twice the RMS current in the normal state in the case of constant loading conditions. As a result, the thermal load on the converter components increases. In addition, this FT implementation approach does not require an additional fuse in series with each semiconductor to isolate the SC semiconductor, where the SC semiconductor is used as the current path. For any fault type in the IB (OCF/SCF), the OB must be reconfigured from the full-bridge rectifier to the Greinacher voltage doubler rectifier using different possible sequences [12]. The FT ZR implementation features thermal loading of components similar to the FT implementation with redundant capacitors but does not use any auxiliary switches.

Currently, this concept was implemented for an SRC-based DC transformer converter. At the same time, its application in IBBC based on quasi-Z-source topologies shows overall efficiency deterioration and possible thermal cycling issues, as described in [14].

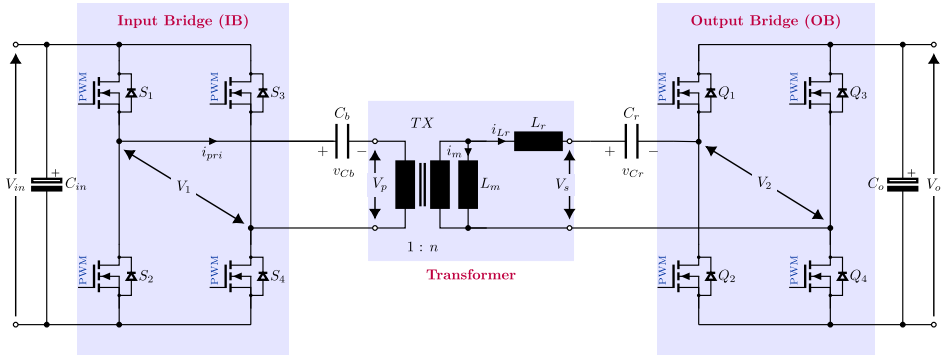


Figure 2.4 A fault-tolerant isolated DC-DC converter with zero-redundant components on the input and output sides.

2.3 Summary

The fault-tolerant implementation approaches have been discussed in the chapter to overcome semiconductor faults in galvanically isolated DC-DC converters based on SRC as the reference topology. Among them, the FT ZR SRC shows low implementation costs but requires power curtailment control if a fault occurs. It must be noted that there is a trade-off between adding additional components to the converter design and the associated increase in the converter size and initial cost needed to maintain the same converter performance before and after a fault. On the other hand, an FT ZR converter could suffer from overloading healthy remaining components after a fault occurs if no power curtailment algorithm is implemented. The FT implementation approach based on topology reconfiguration with zero redundancy is beneficial in cost-sensitive applications. The performance of the proposed FT ZR implementation provides the same post-fault stress of the components as the FT implementation with redundant capacitors. However, the reconfigurable FT ZR-SRC does not need auxiliary switches. Therefore, it can achieve a better cost-performance trade-off in FT converters.

This chapter shows the research gap in FT IBBCs with zero redundancy, which was solved in this work. In addition, it establishes the need for power curtailment control techniques and appropriate methodology for lifetime analysis of the galvanically isolated DC-DC converters.

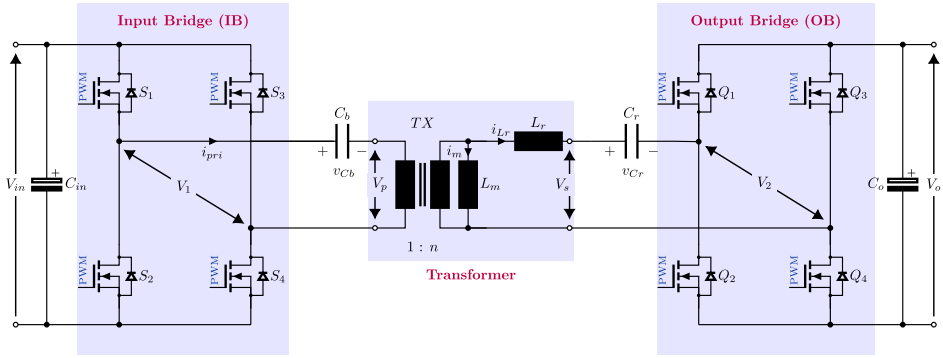
3 Proposed Fault-Tolerant Zero-Redundancy Series Resonant Converter

3.1 Topology Description

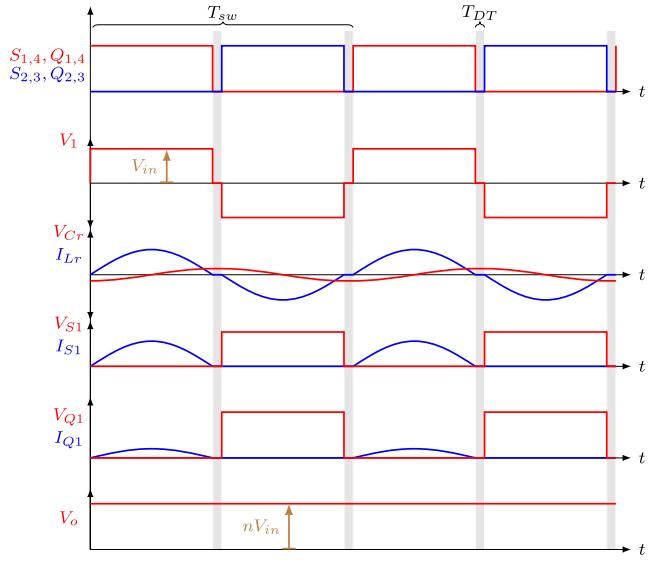
The basic structure of the proposed isolated buck-boost converter is provided in Figure 3.1(a). It contains only two hybrid switching bridges at the input and output and can be reconfigured from full- to half-bridge after a fault is detected. The blocking capacitor C_b contributes to avoiding the DC bias in the transformer current, which helps to avoid saturation of the transformer core after reconfiguration. In addition, C_b has a high capacitance value not to affect the IBBC resonant frequency. The idealized steady-state waveforms of the IBBC during the normal state are depicted in Figure 3.1(b), in which the IBBC is operating as a typically full-bridge SRC in the IB with a synchronous rectifier in the OB.

During the post-fault operation, for example, SCF at S_4, as shown in Figure 3.2(a), the average voltage across C_b and C_r equals half of the input and output voltages, respectively (see Figure 3.2(b)). Therefore, the total gain of the converter before and after the failure and consequent topology reconfiguration remains unchanged. It features direct power transfer into the load during most of the switching period. The primary side of the isolation transformer is coupled with an active full/half-bridge inverter. The semiconductors of the primary side bridge in the same leg are complementary and turned on with a short dead time in order to avoid a supply short-circuit. With this pulse width modulation (PWM) for the IB, the circulating current and conduction losses are minimized, and the primary side semiconductors are turned on with zero voltage switching (ZVS). With proper magnetic integration, the SRC utilizes the leakage inductance of the transformer, TX, as a part of the resonance tank to reduce the cost and size of the target converter.

One of the main drawbacks of SRC-based converters is the high voltage stress of the resonant capacitor in case of overloads, short-circuited output terminals, SCFs on the output side, or fast load transients. Depending on applications, this topology could be implemented with a slightly modified rectifier circuit that clamps the voltage of the resonant capacitor at the expense of somewhat higher losses, as was demonstrated in [PAPER-IV].

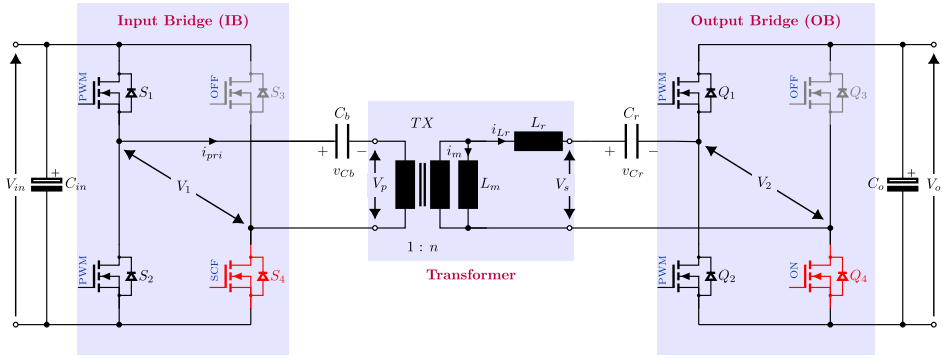


(a)

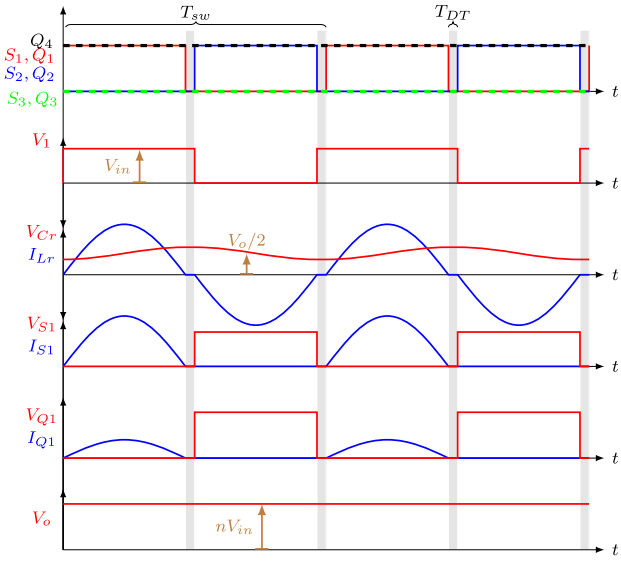


(b)

Figure 3.1 The FT ZR-SRC: primary circuit (a) and idealized steady-state waveforms during normal operation (b).



(a)



(b)

Figure 3.2 Post-fault operation of the FT ZR-SRC: an example of a possible reconfiguration after the fault in the MOSFET switch S_4 (a) and idealized steady-state waveforms during post-fault operation (b).

3.2 Modulation Techniques

As mentioned earlier, the studied FT ZR-SRC belongs to the IBBC family and can regulate the input voltage in a wide range. It operates at a fixed switching frequency and maintains its buck-boost voltage regulation functionality after a fault. This thesis considers it in low-power PV applications, where its compact design with a small (integrated) resonant inductor is beneficial. Although such an implementation results in low values of the quality factor of the resonant tank, the dc voltage gain can be controlled using pulse width modulation at a fixed switching frequency, simplifying the converter design.

In the literature, there are different PWM techniques for the SRC operating with a low-quality factor at a fixed switching frequency, such as phase-shift modulation (PSM) [17], asymmetric PWM (APWM) [18], interleaved PWM [19], and forced half resonance (FHR) [20]. The steady-state waveforms of the FT ZR-SRC using these PWM techniques

are depicted in Figure 3.3. The two former PWM techniques are used for buck operation when the PV voltage exceeds the nominal value by adjusting the phase shift between the two legs of the IB inverter. The PSM in Figure 3.3(a) is applied in the case of the full-bridge operation of the IB inverter. The APWM in Figure 3.3(b) is employed in the case of the half-bridge operation of the IB inverter.

On the other hand, the OB transistors need to short-circuit the secondary winding to step up the voltage when the PV voltage is below the nominal value. Two PWM techniques are employed: interleaved modulation from Figure 3.3(c) to implement a full-bridge boost rectifier and forced half-resonance modulation from Figure 3.3(d) to implement a boost voltage doubler rectifier. After the resonant inductor is charged with additional energy from the input side, it releases this stored energy to the load. The corresponding state-plane trajectories of these four PWM techniques are shown in Figure 3.4, in which V_o is the converter output voltage, and Z_r is the resonant impedance.

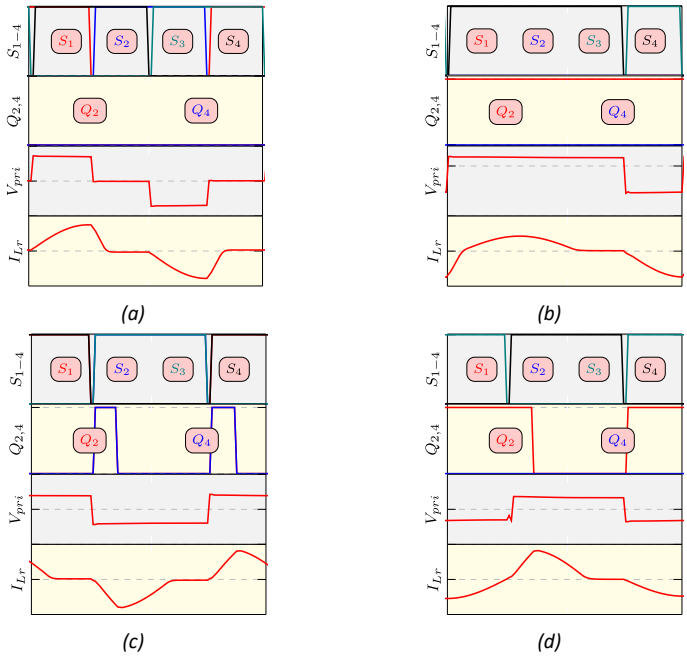


Figure 3.3 Steady-state waveforms of ZR-SRC in normal operation for one switching period at different PWM methods: FB-FB with buck operation (PSM) (a), HB-HB with buck operation (APWM) (b), FB-FB with boost operation (Interleaved modulation) (c), and HB-HB with boost operation (Forced half-resonance) (d).

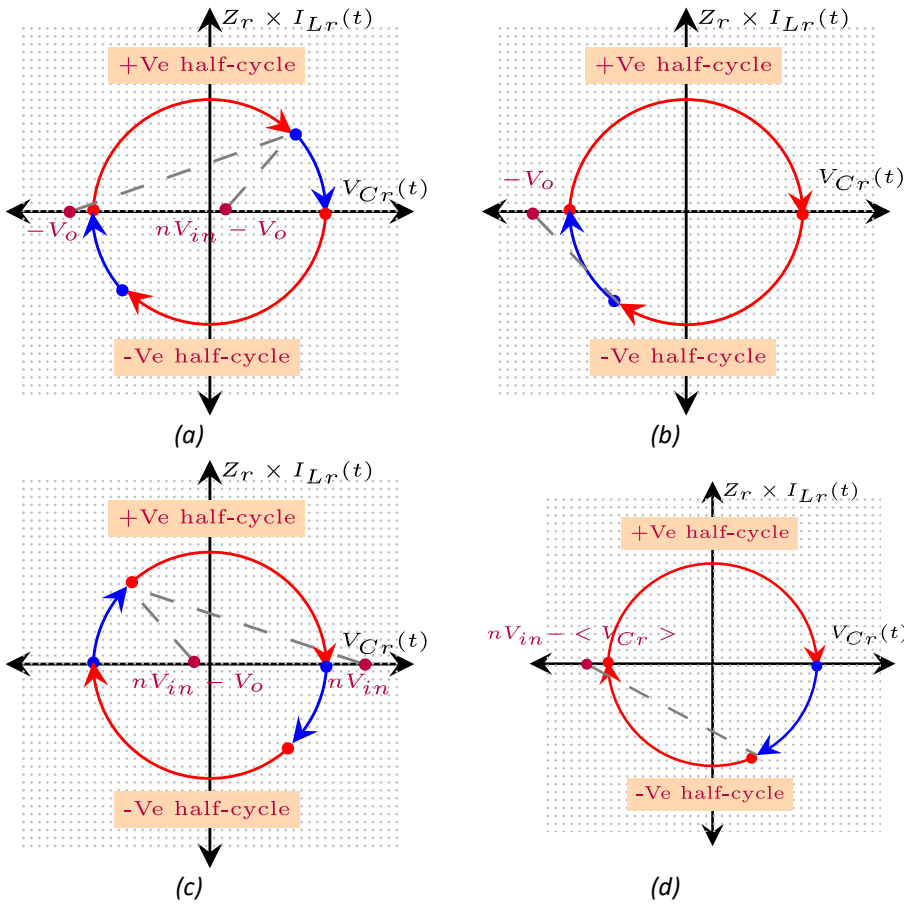


Figure 3.4 State-plane trajectory of the resonant tank variables at different PWM techniques: PSM (a), APWM (b), Interleaved PWM (c), and forced half-resonance PWM (d).

3.3 Characteristics at Post-Fault Operation

As discussed in previous chapters, the FT ZR-SRC employs a faulty short-circuit switch as a current conducting path to reconfigure the faulty bridge from full-bridge to half-bridge operation. Consequently, laboratory tests were3 conducted to investigate the performance of the short-circuited faulty switches and the resulting converter efficiency. The test results are given in [PAPER-II].

This part investigates the distribution of the fault types in MOSFETs in the FT ZR-SRC. To this end, several defective MOSFETs are eventually soldered into actual prototypes operating at the fixed switching frequency close to 100 kHz. The selected batch considers Si MOSFETs for the IB and SiC MOSFETs for the OB. One phenomenon that has been observed is that surface-mounted Si devices maintain mechanical integrity after a fault. Contrary to this, SiC devices working at the high-voltage side could explode, destroying the case integrity and evaporating the semiconductor crystal inside, as demonstrated in Figure 3.5. An explosion of SiC devices results in OCF in all observed cases. On the other hand, the SiC MOSFETs maintain mechanical integrity without any visible damage in the case of an SCF.

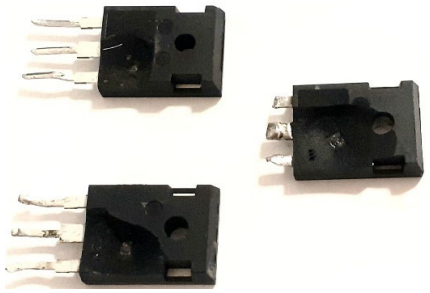


Figure 3.5 Example of case damage to a SiC MOSFET featuring OCF.

The obtained results demonstrated that the SCF stands for 100% of the collected samples of low-voltage Si MOSFETs, and the main reason behind this could be the high current stress on the low-voltage side. Additionally, an 18/82% distribution between OCF and SCF was found for the high-voltage SiC MOSFETs in the OB of the ZR-SRC topology. This necessitates detecting and identifying both fault types in the OB but only SCFs in the IB of the proposed FT ZR-SRC converter.

Short-circuited MOSFETs must be analyzed regarding impedance behavior to prove the feasibility of using a short-circuited MOSFET as a current conduction path after a fault. Different faulty MOSFETs were subjected to maximum current stress and fixed-switching operation for 40 hours, and their resistance remained unchanged. The post-SCF resistance of Si MOSFETs is usually below 100 mΩ. One of the tested samples with a post-fault resistance of 7 mΩ is shown in Figure 3.6(a) as a typical case. A few samples showed post-SCF resistance in the range of 30-90 mΩ. For example, the measurement results for one such device are shown in Figure 3.6(b). Hence, Si MOSFETs, the most fragile component in the converter according to the survey in [8], could be used as a conduction path with negligible resistance after an SCF.

A somewhat different situation was observed in the case of SiC MOSFETs featuring an SCF. Most cases show nearly ideal short-circuit with post-SCF resistance values of much below normal $R_{ds,on}$ as shown in Figure 3.6(c). On the other hand, as exemplified in Figure 3.6(c), several cases show post-SCF resistances that are one order of magnitude higher than normal $R_{ds,on}$. This faulty switch with high post-SCF resistance was tested under load conditions for 30 hours at 2 A. Its resistance changed from 36.8 Ω to 41.20 Ω. The literature indicates that such a MOSFET would eventually converge to SCF or OCF.

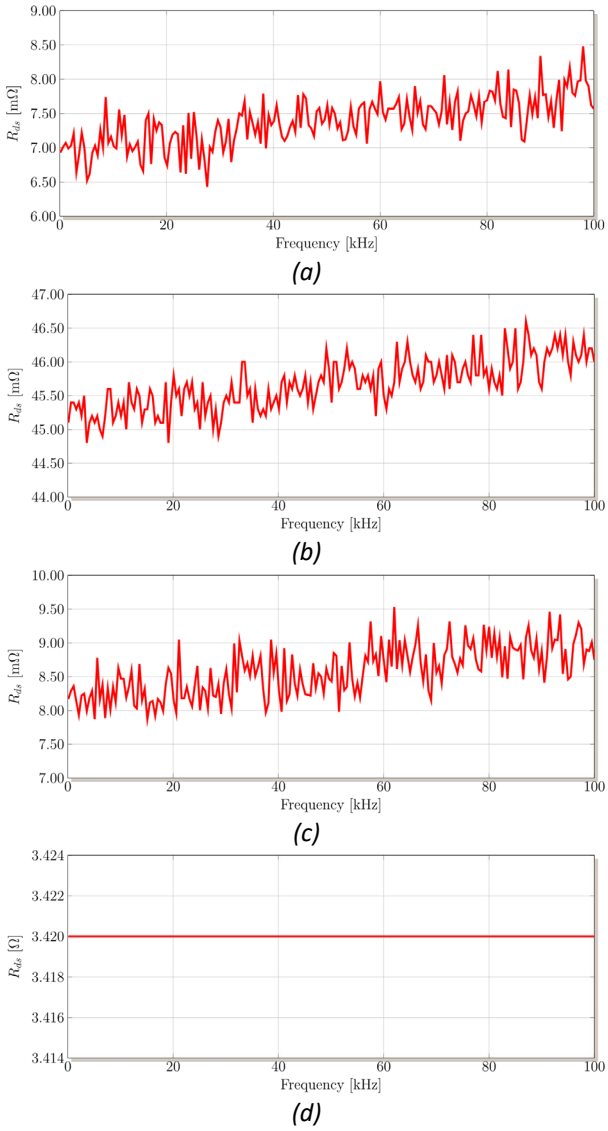


Figure 3.6 Post-SCF drain-source resistance measurement results of four failed MOSFETs: low-resistance Si (a), high-resistance Si (b), low-resistance SiC (c), and high-resistance SiC (d).

3.4 Fault Detection Issues

To address power converter failures, the fault must first be detected using an appropriate signature signal that adequately describes the converter's operation in every state. In addition, the fault location may need to be defined in order to decide whether to reconfigure the converter after the signature signal triggers the failure mode. The diagnosis signal, i.e., the signature signal, should provide enough information about the converter operation during both the normal and faulty state. When dealing with the fault in the converter, it comprises the fault diagnosis and the fault remedial, i.e., fault-tolerance, to ensure that the converter continues operation even in the faulty state. The fault diagnosis stage includes detecting that the converter enters an abnormal

condition, and sometimes it provides localization of the defective component in the converter. The primary purpose of the fault remedial is to make the converter operation continue despite the possibility of reduced performance.

Generally, diagnosis methods can be broken into signal and model-based methods [21]-[22]. With the model-based methods, the actual values of the converter diagnosis signals are measured and then compared with the observed values based on approximators. The most well-known approaches for estimation are the Kalman filter [23], extended Kalman filter [24], slide mode observer [25], and Luenberger observer [26]. The converter state, i.e., normal or faulty, can be identified based on the deviation between the measured and estimated values. On the other hand, the signal-based methods can be classified into time-domain and frequency-domain analysis of the diagnosis signal. The time-domain methods use a simple and low-cost analog implementation to compare the diagnosis signals with a threshold level [27]-[28]. The latter analysis depends on using Fourier Fast Transform (FFT) to extract the primary information from the diagnosis signal to define the converter status [29]-[30]. On the other hand, the frequency-domain analysis has the drawback of high computational effort and complexity.

The voltage of the resonant inductor could be used as a signature signal for short-circuit detection, as proposed in [PAPER-III]. The method does not require expensive components as it can utilize a small tertiary winding for sensing this voltage. The high speed of detection achieved results from the operation of the resonant tank, which experiences much higher stress of components after a fault.

3.5 Summary

This chapter addressed two hypotheses set forth in this thesis. First, the ZR FT IBBC was proposed based on the SRC topology. The proposed converter is capable of input voltage regulation in a wide range, both before and after a semiconductor fault. This concept creates new opportunities in cost-sensitive applications, where fault tolerance is typically avoided as it penalizes the implementation cost. Second, it was demonstrated that using a defective switch as a current conducting path in a reconfigurable FT DC-DC converter has proven feasible. This makes the ZR fault tolerance concept feasible and practical. As a result, it is possible to tolerate the failure of one of the DC-DC converter switches without affecting the overall operation of the converter. However, a converter of this type must be thermally engineered to withstand possible high ohmic losses in short-circuited MOSFETs. High ohmic losses can cause the converter to heat up and fail again if the thermal design does not consider this issue. As an alternative, its control system could include a power curtailment algorithm that limits the stresses on the remaining healthy components after a fault. This approach also diminishes the risk of overheating a short-circuited switch that serves as a current conductor in a reconfigured DC-DC converter.

4 Reliability-Oriented Design of the SRC-Based Fault-tolerant DC-DC converter with Zero Redundancy

4.1 Converter Lifecycle and Reliability

The most well-known definition of reliability from an engineering point of view is "the probability that an item will perform a required function without failure under the stated conditions for a stated period of time" [31]. To quantify the reliability, the component's hazard rate (i.e., failure rate) λ denotes the conditional likelihood that the component fails in a time interval. There are three main regions in the lifetime of electronic devices: early infant mortality failure, constant random failure, and wear-out failure, as shown in the classical life cycle bathtub curve in Figure 4.1 [32]. To prevent early life failures, burn-in or screening tests may be used.

Random failures of components play a vital role in determining the probability of a system failure. The wearing out of components dominates over the probability of random failures as the service life increases, particularly at the late stages of useful life. Generally, power semiconductors fail in two ways: catastrophically with constant failure rates and wear out with variable failure rates over time. Both have different failure mechanisms, as shown in Figure 4.2. Since power electronic converters are typically long-lived in practice, they are assumed to operate in the useful lifetime range in many engineering applications [33]-[35]. Due to the lack of 100/120 Hz power ripple in the considered DC-coupled applications, the wear-out failures are ignored in this case study, and only random failures are considered [PAPER-VI], [33].

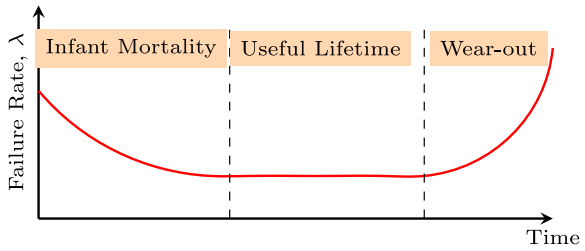


Figure 4.1 The typical lifecycle bathtub curve of an item.

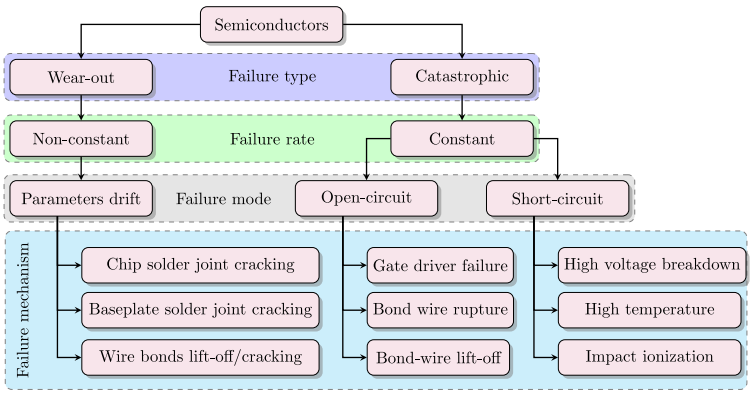


Figure 4.2 The modes and mechanism of power device failures [34]-[35].

4.2 Synthesis of High-Resolution Application-Specific Mission Profile

The reliability of installed photovoltaic systems has become a significant problem as the use of renewable energy in utility services has increased, causing concerns about possible power outages. The mission profile of incident solar irradiance and ambient temperature significantly affect solar PV output power. In addition, the mission profile of the operating conditions is required to analyze the PV system behavior for reliability prediction and system-level availability or to forecast the energy yield for a specific long-term horizon. The time step or resolution of the mission profile dataset depends on several elements, including the installation environment, the capacity of the dataset, and the implementation costs [PAPER-V]. Data loggers are required to capture the environmental data with appropriate precision to collect the mission profile at a high resolution, which could be costly [36]. In [37], it was examined how the resolution of the mission profile affected the reliability forecast and the lifetime consumption of PV inverter semiconductors. The findings of this study indicated that the low resolution of a mission profile could lead to an overestimation of the PV inverter lifetime. The mission profile resolution significantly impacts the prediction of the accumulated damage, particularly in cloudy environments. Figure 4.3 shows the yearly mission profile used in this study. It is captured for Northern Denmark (Aalborg) with a resolution of one second and a total of 31'863'123 records. The mean solar irradiance between November and February is low, impacting the temperature profiles of the IBBC components.

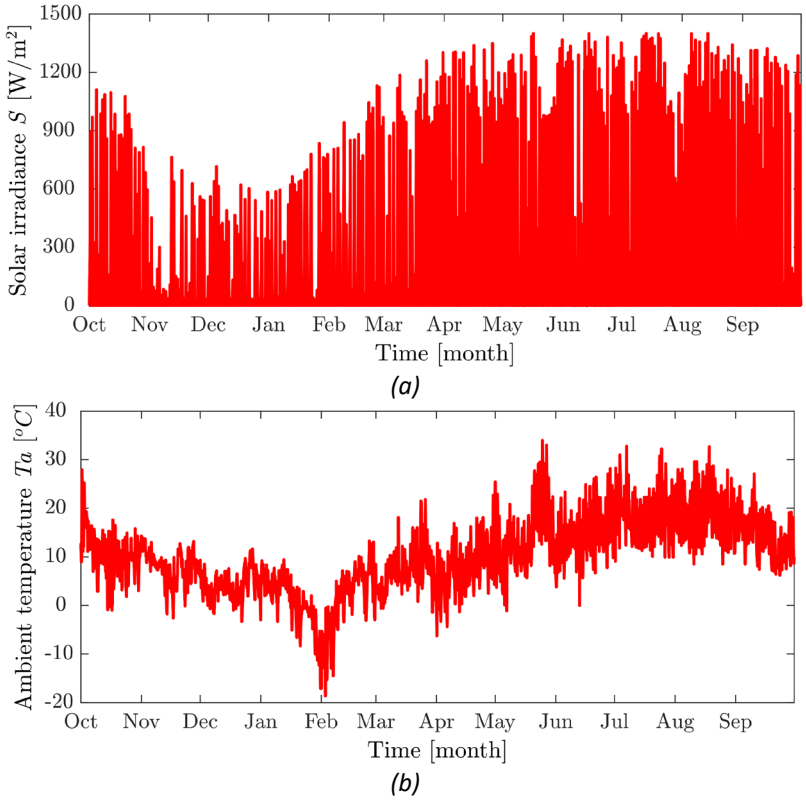


Figure 4.3 The yearly mission profile for Aalborg, Denmark, solar irradiation (a) and ambient temperature (b).

Figure 4.4 shows the solar irradiance for a clear and cloudy day at various resolutions of the mission profile. It is evident that the resolution of the solar irradiance profile has little impact on the clear-day mission profile when the solar irradiance has a minimal dynamic change. On the other hand, the dynamic change in solar irradiance deviates slightly from the mission profile resolution, particularly for a cloudy environment.

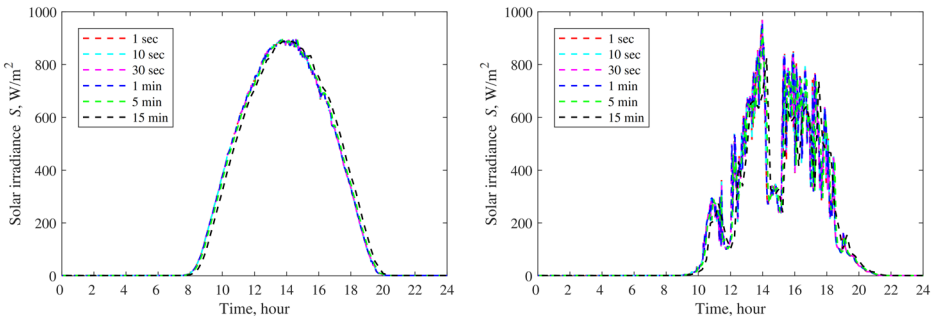


Figure 4.4 The daily solar irradiation at different mission profile resolutions, clear day (a) and cloudy day (b).

Table 4.1 provides the annual energy yield estimation results for a 60-cell Si PV module at different resolutions. The PV module's overall energy (kWh) is roughly the same for any resolution considered. Less than 0.5% separates the predicted energy yield values. The effectiveness of Python and MATLAB, the two popular software frameworks used to solve this kind of computational problem, were compared. For various mission profile resolutions, the computing time for both the Python and MATLAB scripts is displayed in Figure 4.5. The algorithm was executed on a personal computer with an Intel® Core™ i5-8265U CPU running and 16 GB of random access memory. The Python environment with C-based libraries offers an advantage in computation speed over MATLAB of between two and over four times. Therefore, the Python environment was used to implement the reliability estimation methods in this thesis to achieve an acceptable execution speed. The advantage of code development in Python becomes even more apparent for the analysis of more complicated converters, like the IBBCs, where a higher number of components should be modeled.

Table 4.1 Prediction of the annual energy yield at different mission profile resolutions.

Resolution	1 s	10 s	30 s	1 min	5 min	15 min
***E*, kWh**	314.0	314.5	314.5	314.6	314.8	315.1

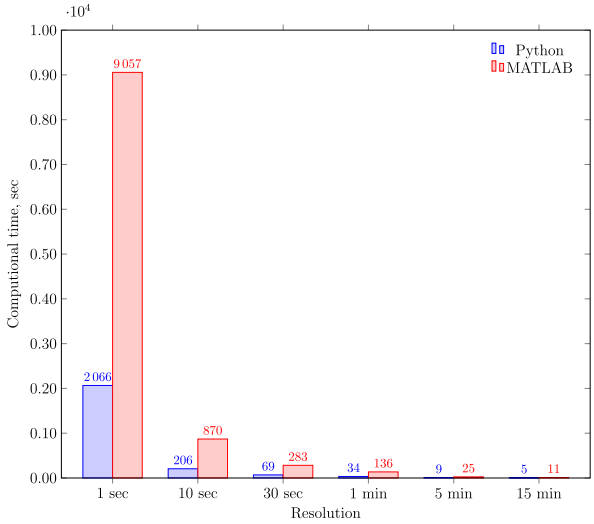


Figure 4.5 Comparison between Python and MATLAB environments regarding execution speed of computational tasks employing high-resolution mission profile.

4.3 Reliability Analysis Frameworks

4.3.1 MIL-HDBK Reliability Handbook

Since the 1990s, the United States Navy has established the MIL-HDBK-217F Handbook, which is regarded as a standard for the reliability prediction of electronic systems [38]. It has been empirically verified that the models of the items inside it are accurate. With the MIL-HDBK-217F handbook, the random failure rate λ of the item can be expressed as a multiplicative form as

$$\lambda = \lambda_b(\prod_{i=1}^{n} \pi_i)\,, \tag{4.1}$$

where λ_b is the basic failure rate, and *n* denotes the number of π-factors of the item, which depends on the item's category. The unit of the resulted λ in this reliability approach is failures/(10^6 hours). The failure rates based on MIL-HDBK-217F associated with the MOSFETs (λ_{MOSFET}) can be defined as in (4.2). For the isolation transformer, its failure rate ($\lambda_{Transformer}$) can be given as in (4.3), while the failure rate of the capacitor ($\lambda_{Capacitor}$) is calculated using (4.4), in which π_C denotes the capacitance stress factor and π_V denotes the voltage stress factor.

$$\lambda_{MOSFET} = \lambda_b \pi_T \pi_A \pi_Q \pi_E\,, \tag{4.2}$$

where π_T is the temperature stress, π_A is the application stress, π_Q denotes the quality factor, and π_E is environmental stress.

$$\lambda_{Transformer} = \lambda_b \pi_T \pi_Q \pi_E \tag{4.3}$$

$$\lambda_{Capacitor} = \lambda_b \pi_T \pi_V \pi_C \pi_Q \pi_E \tag{4.4}$$

4.3.2 FIDES Reliability Guide

Eight French companies created the FIDES dependability manual guideline in its initial form in 2004 and revised it in 2009 [38][39]. The 2022 updated version is scheduled for publication in 2023. In the FIDES Guide, the component's random failure rate represented by the unit of FIT (i.e., failure per 10^9 hours) is predicted by considering the physics of failures. Here, the failure rate is expected to remain constant throughout the product's useful life, and the wear-out phase will not begin while the mission profile exists [39]. Since the component's useful lifetime is being modeled, it is not possible to assess the component's reliability during startup by using the FIDES Guide [40].

In contrast to the MIL-HDBK-217F reliability handbook, the FIDES reliability guide considers device technology, the impact of the extrinsic failure rate, and the sensitivity to quality parameters from design to usage. It employs the yearly mission profile for the item under consideration. Each mission profile can be subdivided into a series of phases, each with a time limit of hours [41]. With this reliability approach, the item failure rate can be expressed in the general form as

$$\lambda = \prod_{PM} \prod_{Process} \lambda_{Phy} \, , \tag{4.5}$$

where $\prod_{PM}$ is the technical and quality while manufacturing the item, $\prod_{Process}$ includes all the stages of the item processes starting from the setting of the specification to the operation in the field and maintenance, and λ_{Phy} is the physical failure rate related to the item that can be calculated using the mission profile. More details can be found in the paper [PAPER-VI].

4.4 Analytical Results of Reliability Prediction

The prediction of *n*-th component reliability over the time *t* can be evaluated after determining its failure rate according to (4.6). The mean time to failure (MTTF), which indicates the time the component takes from the beginning to work until the first failure occurrence, can be computed using (4.7). The complete flowchart for the reliability evaluation of the studied IBBC FT ZR-SRC is shown in Figure 4.6. After reading the photovoltaic mission profile comprising the solar irradiance *S* and the ambient temperature T_a, the thermal stress of the IBBC components could be determined using the look-up table synthesized from the simulation of power losses in PLECS. The complete mathematical thermal analysis for each component of the SRC-based IBBC is detailed in Section III of [PAPER-VI]. The rainflow counting algorithm is used to manage the non-uniform thermal profile of the IBBC components and define the peak-to-peak thermal cycle, the mean temperature of the cycle, and the cycle duration [42]. In the current case study, the reliability block diagram is examined in a series connection, whereby if one component fails, the IBBC converter enters the faulty state. As a result, the IBBC failure rate can be expressed as in (4.8), where $N = 11$ denotes the number of IBBC key components considered. The reliability of the IBBC can therefore be determined by taking into account the product of the reliability of the system components as in (4.9).

$$R_n(t) = e^{\lambda_n t} \tag{4.6}$$

$$MTTF = 1/\lambda_n \tag{4.7}$$

$$\lambda_{IBBC} = \sum_{n=1}^{N} \lambda_n \tag{4.8}$$

$$R_{IBBC}(t) = \prod_{n=1}^{N} R_n(t) \; = e^{\lambda_{IBBC} t} \tag{4.9}$$

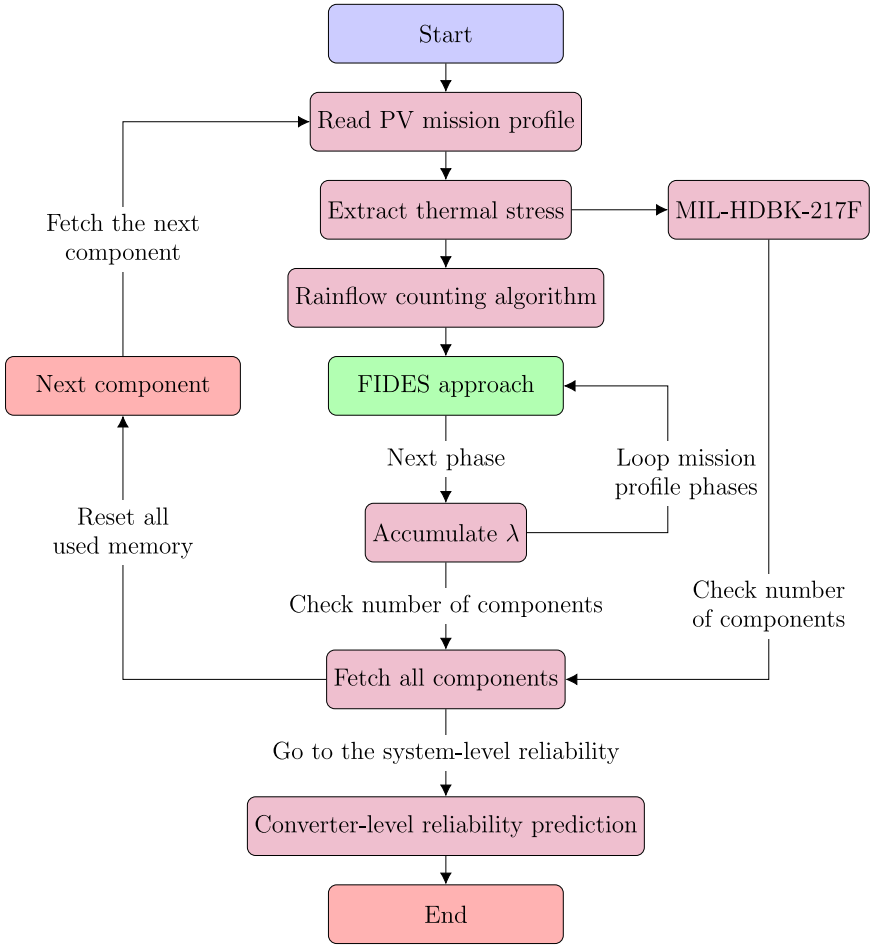


Figure 4.6 The procedure of IBBC reliability prediction from the component level to the system level.

The failure rate from the two reliability analysis approaches for each IBBC component is shown in Figure 4.7(a). For MIL-HDBK-217F, it is clear that the $S_{1\text{-}2}$ features the highest failure rate among the FT ZR-SRC components. On the other hand, the transformer has the highest failure rate for the FIDES Guide-based analysis due to the relatively high basic failure rate of 0.125 FIT defined in the FIDES Guide 2009. Therefore, the total failure rate of FT ZR-SRC expressed in failures per year equals 0.0071 and 0.0045 for MIL-HDBK-217F Handbook and FIDES Guide, respectively. Figure 4.7(b) illustrates the reliability prediction of the IBBC over time. The converter starts with 100% reliability, which degrades gradually over time with differing results for the 10% reliability reduction time (B_{10}) of 14.80 and 23.20 years for the MIL-HDBK-217F Handbook and FIDES Guide, respectively. According to the results, the IBBC-based PV system is 83% and 89% reliable after 25 years of operation under the Aalborg mission profile when using MIL-HDBK-217F Handbook and FIDES Guide for analysis, respectively. This asserts that the MIL-HDBK-217F Handbook yields an overdesigned converter with a higher cost due to considering constant worse-case random failure rates.

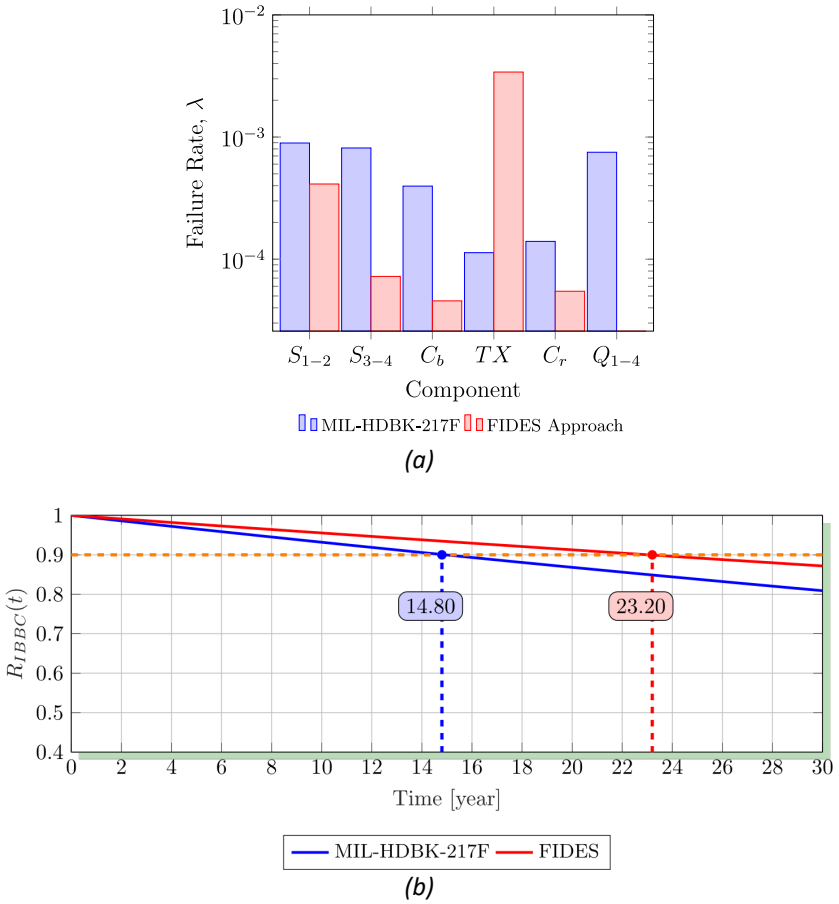


Figure 4.7 Reliability analysis results for IBBC, the annual failure rate of components (a), and reliability prediction of the IBBC over time (b) [PAPER-VI].

4.5 Summary

The main finding in this chapter is the reliability analysis methodology based on the FIDES Guide that considers the actual mission profile discovered in the field. This is important because it ensures that the mission profile is optimally executed, while it is not considered in the method described in the MIL-HDBK-217F Handbook. As a result, it could be concluded that the FIDES Guide, based on established empirical models for the PV converter based on the IBBC, offers a more accurate lifetime forecast and enables the application-tailored design of the DC-DC converter. The results support the fundamental hypothesis that the system random failure rate is primarily caused by the primary-side semiconductors, with the output-side switches having little bearing. The transformer is the least reliable passive component in the IBBC for PV applications because of the high basic failure rate introduced by the FIDES Guide, which cannot be diminished by control or transformer design. In contrast to the reliability analysis, the PV energy forecast does not need a high-resolution mission profile. Finally, the Python environment is regarded as the ideal choice for high-speed execution to examine the reliability of DC-DC converters when using a high-resolution mission profile.

The results obtained prove the third hypothesis of this thesis.

5 Self-Healing Fault-Tolerant PV Microconverter

Self-healing FT ZR-SRC aimed at residential PV module-level applications was proposed in [PAPER-VII]. The complete configuration of the converter considering the fault diagnosis signals is shown in Figure 5.1. It employs a maximum power point tracking algorithm to ensure PV module performance at the maximum power point. The studied converter can achieve the global MPPT. Due to its simplicity, the perturb and observe (P&O) algorithm was utilized for MPPT near the global maximum. The FT ZR-SRC interfaces a residential PV module with a dc microgrid with high capacitance and stiff-voltage V_{MG}. In the normal operation of the converter, the body diodes of the top switches (Q_1 and Q_3) are used as rectifiers.

Moreover, these MOSFETs are used to restore converter operation in the case of an OCF or SCF in the bottom MOSFETs (Q_2 or Q_4). The synchronous rectification is not applied here to avoid degradation of the gate oxide layer in the top MOSFETs Q_1 and Q_3, which strongly depends on the gate voltage stress. In addition, when the converter is operating in the normal state with boost mode, non-overlapping PWM is used to drive the bottom switches of the OB because it provides the best voltage regulation performance at the cost of a slightly lower efficiency [46]. The IBBC design guidelines are provided in this chapter, and the new fault diagnosis and detection methods are discussed.

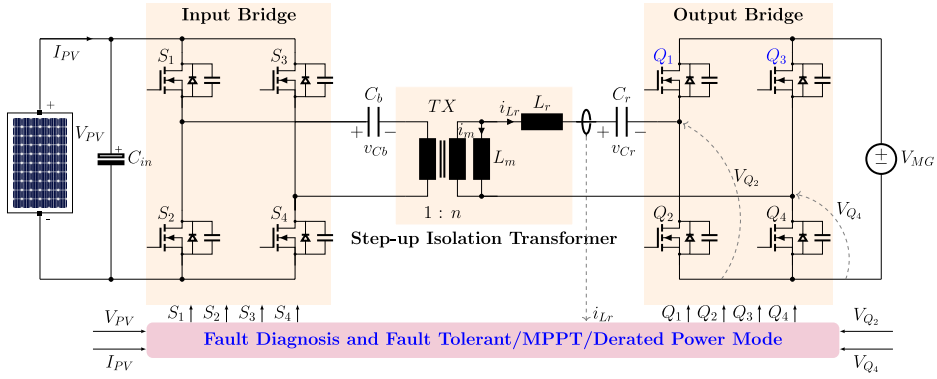


Figure 5.1 Topology of the self-healing ZR-SRC for residential PV coupled with a stiff MG on the output side, considering the measurement signals for MPPT and fault diagnosis.

5.1 Design Guidelines for PV Applications

This subchapter explains how the design guildies for ZR-SRC described in [PAPER-VII] provide good buck-boost voltage regulation performance under all operating conditions. The main goal of the design guidelines is to produce self-healing converters possible with adequate efficiency while still meeting the cost and power requirements.

First, the transformer turns ratio (n) is selected so that the FT ZR-SRC can generate the desired output voltage of 350 V, which is the most common dc-bus voltage for the residential DC MGs (i.e., V_{MG}), at the nominal input voltage of 30 V ($V_{IN,Nom}$) that is typical for 60-cell Si PV modules as in (5.1). This is the most probable operating point of the converter. The converter must provide the best performance at this point. To select the number of turns of the primary winding (that is to say, the low voltage side here), the maximum flux density of the core must be lower than 120 mT at the maximum input voltage according to (5.2), which ensures an acceptable level of losses in ferrite cores.

$$n = \frac{V_{MG}}{2V_{IN,Nom}}, \tag{5.1}$$

$$\Delta B = \frac{V_{IN}}{2N_p A_c}, \tag{5.2}$$

where ΔB denotes the peak-to-peak flux density in the transformer core, N_p is the number of primary winding turns, and A_c is the cross-sectional area of the magnetic core.

The resonant inductance of the SRC should be sufficiently large to minimize the converter losses and thus improve efficiency [43]. The relationship between the resonant inductance L_r and the ZR-SRC power losses must be considered when designing the resonant tank, as shown in Figure 5.2. Increasing the resonant inductance can reduce the converter losses. On the other hand, the ZR-SRC should operate in the discontinuous resonant current mode with a resonant tank quality factor of below one. Hence, the design of L_r is considered a trade-off that should be satisfactory (5.3). To account for losses and non-modeled dynamics in the converter, it might be recommended that L_r is selected in the range of 60-70% of the critical value in (5.3). The value of the resonant inductance in the current thesis is selected at 100 µH.

$$L_r < \frac{2n^2 V_{IN,min} F_{sw}}{I_{IN,max}\omega_r^2}, \tag{5.3}$$

where $V_{IN,min}$ is the minimum input voltage, $I_{IN,max}$ is the maximum input current, and ω_r is the resonant angular frequency.

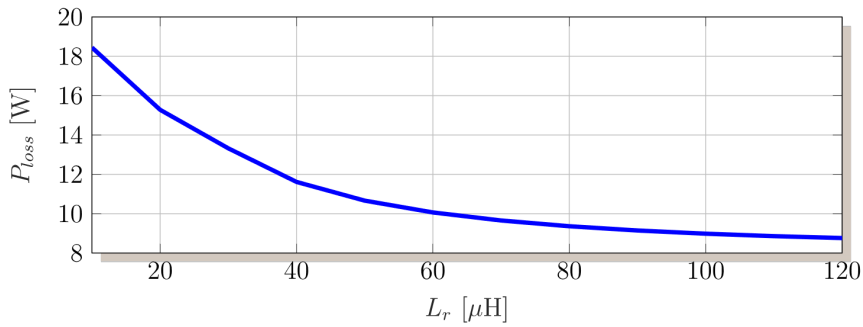


Figure 5.2 The effect of the resonance inductance value on the total power loss of the FT ZR-SRC.

The peak value of the magnetizing current is achieved during the dead-time. It is reflected to the primary winding and recharges the parasitic output capacitance of the semiconductors in the IB. The magnetizing inductance L_m should be designed to allow the magnetizing current to fully charge and discharge the parasitic output capacitances (C_{oss}) of the primary semiconductor during the dead-time (T_{DT}) in the gating signals of the primary switches [PAPER-IV], as

$$L_m \leq \frac{n^2 T_{DT}}{8F_{sw}C_{oss}}. \tag{5.4}$$

The resonant inductance can be implemented as a discrete inductor or integrated into the isolation transformer. The use of the magnetic integration concept has the merit of reducing the converter size and the cost, but on the other hand, the design becomes a challenging task. An isolation transformer with integrated magnetic elements was implemented in this work Using the guidelines given in [44].

The parameters of the resonant tank determine the resonance frequency. To obtain the best conversion efficiency of the converter, it is essential to design the FT ZR-SRC to operate close to the resonant frequency. The resonant capacitor C_r can be directly defined using the specified value of L_r and the resonant frequency F_r using (2.1). According to the circuit configuration, the average voltage of the resonant capacitor equals zero in the full-bridge rectifier for normal operation. It has a dc bias in the half-bridge rectifier configuration for the post-fault operation. The peak-to-peak ripple across C_r (ΔV_{Cr}) is only affected by the output power of the converter P_{out} and the input voltage equal to the voltage of the PV module V_{PV}, as

$$\Delta V_{Cr} = \frac{P_{out} T_{sw}}{2nV_{PV} C_r}, \tag{5.5}$$

where T_{sw} is the switching period.

For the semiconductors of the FT ZR-SRC, the maximum voltage stress of the MOSFETs in the IB equals the maximum open-circuit voltage of the PV module. In contrast, the voltage stress of the OB MOSFETs equals the maximum DC microgrid voltage. Considering expectations of low implementation cost for residential PV converters, the current stress of the IB/OB MOSFETs is designed for normal operation, as provided in [45].

5.2 Fault Diagnosis and Detection Methods

Irrespective of the failure mechanism that leads to a catastrophic failure, the failure mode of the semiconductors (Si MOSFETs in the IB and SiC MOSFETs in the OB) is considered as either OCF or SCF. Generally, resonant topologies are more promising DC-DC converters for the industry. They are widely adopted in many industrial applications, such as data centers and battery chargers, due to their soft switching and high-efficiency features [46]. A recent survey regarding the failure of these converters [8] was conducted among scientists working in the industrial sector and academic positions related to applied power electronics. This provides some variety in the replies collected worldwide and thus increases the accuracy of survey results. Around 72% of the participating companies have more than ten years of market experience. The summary of this detailed survey indicates that the primary semiconductors of the SRC/LLC converters are regarded as the primary source of converter failure. It contributes approximately half (i.e., 47.6%) of the damage source of the converter. Moreover, the survey shows that primary semiconductors fail in the form of SCFs, according to the participant's experience.

Furthermore, several tens of random samples of low-voltage switches that failed while testing high step-up DC-DC converters were collected [PAPER-II]. The quantitative results prove that the SCF fits 100% of the collected dataset. Thus, the resulting statistical analysis of the collected dataset is consistent with the statistical results collected for the SRCs in industrial applications [8]. Hence, in line with the previous discussion, this study only considers the SCF of the primary semiconductors during fault diagnosis and detection. OCF and SCF are considered for the OB rectifier to provide a comprehensive fault study on the FT ZR-SRC topology.

5.2.1 SCF of the Primary-Side MOSFETs

Since a PV module feeds the input of the FT ZR-SRC, both the PV module voltage and current are required data for the MPPT (i.e., V_{PV} and I_{PV}, respectively). The PV is a controlled current source that does not have an excessively high short-circuit current compared to the current at the MPP. Hence, in the case of fast detection of a random fault, the SCF in one of the IB MOSFETs cannot harm the IB MOSFETs. Using existing measurement signals to diagnose faults in input-side MOSFETs avoids the additional cost and size of including additional sensing components, which is the key distinguishing feature of the proposed fault diagnosis method. Specifically, the PV voltage is employed as the diagnosis signal to detect the SCF in the front-end inverter MOSFETs. When one of the IB switches experiences SCF, the PV voltage begins to fall from the V_{MPP} to zero in a period influenced by the PV module capacitance and the drain-sources resistance of the defective and healthy switches in the same leg. The healthy switch is turned on under the specific modulation signal, short-circuiting the input. As a result of an SCF, the significant variation in the PV voltage indicates that the IB switches are malfunctioning.

Once the SCF fault has triggered the diagnosis algorithm, its precise location in the left or right leg should be determined. As the defective leg becomes inactive and cannot receive any switching signal, it is not always possible to precisely identify which MOSFET in the IB is defective. It is worth noting that with the proposed algorithm, there is no need to define the switch itself accurately. Only the faulty leg should be identified (i.e., left or right leg). In further discussion, it is assumed that the left leg had suffered SCF, so both gate signals of switches S_1 and S_2 should have their gating signals disabled. After a brief period, in the order of milliseconds, the PV voltage should be measured to verify its value. In this manner, it is unnecessary to check the sign of the primary voltage or incorporate the logical switching signals of the switches into the detection routine. The design of a fault detection routine is subsequently made simpler and more feasible. The SCF diagnosis and detection process in IB MOSFETs is depicted in Figure 5.3.

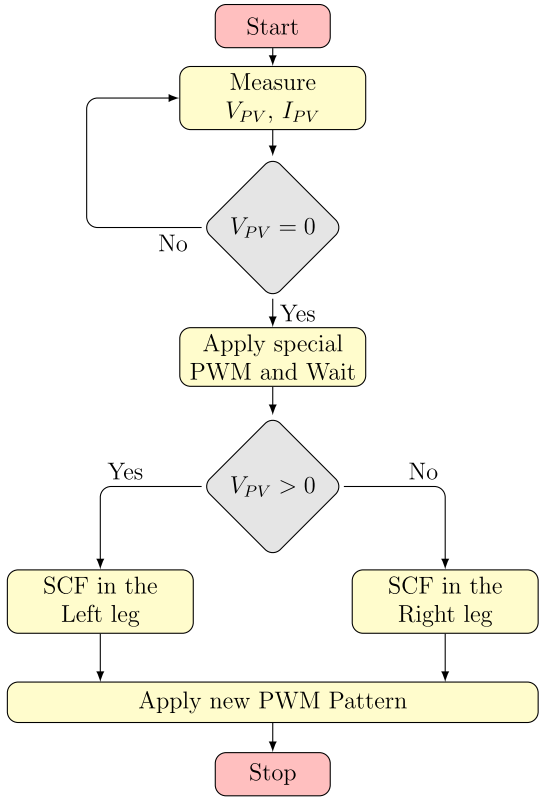


Figure 5.3 Flowchart of diagnosing and detecting the SCF of IB MOSFETs.

5.2.2 OCF of the Secondary-side MOSFETs

The voltage of the bottom switches is sensed (i.e., V_{Q2} and V_{Q4} are the drain-source voltage of the switch Q_2 and Q_4, respectively), as shown in Figure 5.4, to determine the OCF in the OB MOSFETs. Since the output voltage of the sensing circuit and the isolated driver of the bottom switches share a common ground, the voltages of the bottom switches were chosen as diagnosis signals. The OCF in the output-side full-bridge MOSFETs causes the resonant current to oscillate around the zero axis because of the parasitic capacitances of the converter semiconductors, which prevent the converter from functioning correctly. In the case of an OCF, the body diode of a defective switch becomes inactive and is no longer functional in the circuit. The bottom switches of the output-side rectifier each have an OCF detection and localization circuit. As a result, it is possible to trigger and identify the OCF in the OB simultaneously.

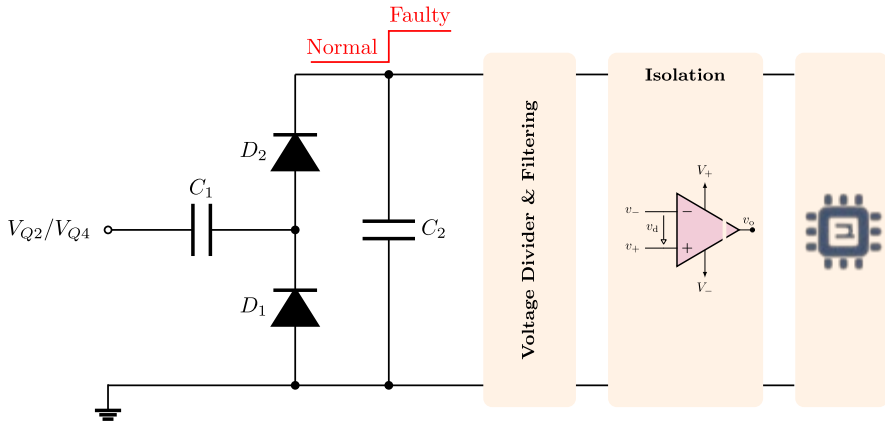


Figure 5.4 The voltage sensing circuit used to diagnose and detect the OCF in each bottom OB switch.

5.2.3 SCF of the Secondary-Side MOSFETs

The resonant inductor current I_{Lr}, which rises when the SCF occurs in one of the OB bottom switches, is used as the signature signal for SCF detection in the OB rectifier. A low-cost current transformer is required to sense I_{Lr} due to the low secondary current of the step-up transformer. It is best to rectify the sensed inductor current using the low-power full-bridge rectifier because it is a bipolar signal. Figure 5.5 depicts the proposed SCF detection algorithm's flowchart.

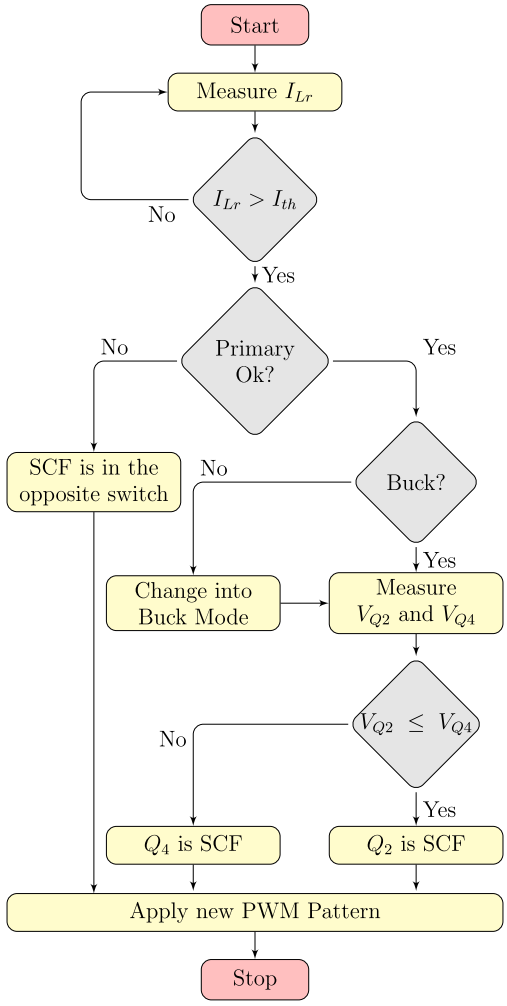


Figure 5.5 Flowchart of diagnosing and identifying the SCF in the OB MOSFETs.

5.3 PV Power Curtailment during Post-Fault Operation

During the FT ZR-SRC post-fault operation, overloading can occur if a residential PV module provides the rated power. The main reason is that the critical components are overloaded when the converter operates close to its rated power. Suppose the FT ZR-SRC continues to handle the same rated power as the normal operation after the fault occurrence. In that case, a catastrophic failure could result from the high thermal stress across the converter component, especially the IB MOSFETs. Considering that the IBBC components are designed for current stress in normal operation, their lifetime could be shortened by delivering the rated power during post-fault operation. A simple technique for increasing the reliability of FT DC-DC converters with minimal redundancy and thus extending their lifetime is to limit the converter input power during PV energy peaks. The estimated random failure rate for the FT PV microconverter under consideration is shown in Figure 5.6(a). The power curtailment level should be set at 200 W to maintain the random failure rate of a healthy microconverter. The failure rate is reduced further when the power curtailment level is reduced to 150 and 100 W.

A healthy FT PV microconverter can harvest 309 kWh/year at the PV terminals, which drops by roughly 12% for the power curtailment at 200 W, as shown in Figure 5.6(b). Given that more energy is produced at higher power levels in southern climates than in the reference scenario from Northern Europe, it is essential to note that the relationship between the curtailment power level and energy yield loss would be much more significant in those regions. Even in the considered northern climate, the designed self-healing PV microconverter would fail due to overheating the remaining healthy semiconductors in subsequent summer (i.e., sunny) months if its input power was not limited.

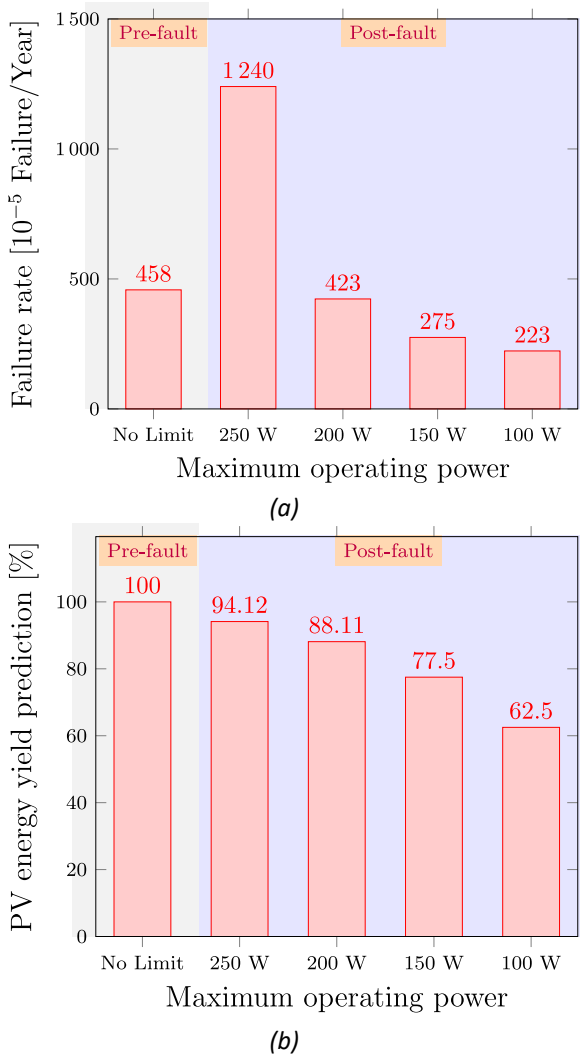


Figure 5.6 Annual failure rate of the FT ZR-SRC PV microconverter before and after the occurrence of a fault with power curtailment (a) and annual PV yield prediction of the FT ZR-SRC PV microconverter for different PV power curtailment levels (b).

During the PV power curtailment operation, the converter input voltage of the self-healing PV microconverter differs from the MPP voltage. This operation could be achieved at two points on the P-V curve, below and above the MPP voltage. Reducing power above the MPP voltage is advantageous because high step-up converters typically offer higher efficiency at lower dc gain [47].

5.4 Experimental Results

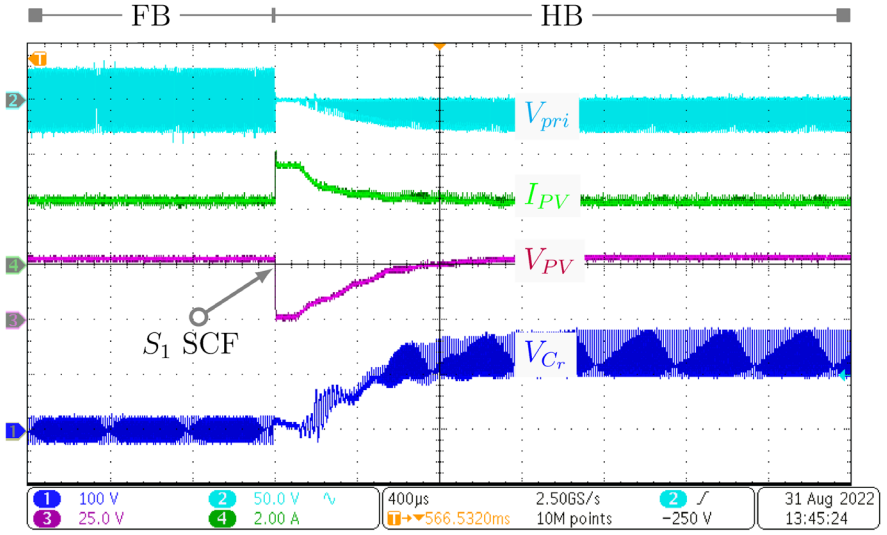
The experimental setup was assembled in the power electronics research laboratory of Tallinn University of Technology using the parameters listed in Table 5.1. The microcontroller STM32F334 has been used to implement the modulation and control algorithms.

The closed-loop control system was implemented to perform a global MPPT. The fault detection and identification routine are run in parallel routines handling interrupts of timers setting the sampling frequency. After a fault is detected, MPPT is disabled for a short time if fault identification is needed. The microconverter recovers its operating point on-the-fly and continues the MPPT. The proposed fault detection and identification methods ensure high-speed SCF detection, while OCF could be detected slower as it would not cause current overstress of the remaining components. This approach achieves a trade-off between performance and the implementation cost of the detection circuitry.

Table 5.1 Parameters and Components of the Prototype in the Laboratory

Parameter	**Designator(s)**	**Value**
PV input voltage range	V_{IN}	10:60 V
PV input max. current	$I_{IN,max}$	10 A
Input side capacitor	C_{IN}	150 µF
Leakage inductance	L_{lk}	100 µH
Magnetizing inductance	L_m	1 mH
Transformer turns ratio	n	12
Resonance capacitor	C_r	33 nF
DC MG voltage	V_{OUT}	350 V
Switching frequency	F_{SW}	95 kHz
Components	**Designator(s)**	**Part Number**
Primary side switches	S_1 … S_4	FDMS86180
Secondary side switches	Q_1 … Q_4	SCT2120AF

First, the proposed fault diagnosis and detection of the ZR-SRC semiconductors are tested. As shown in Figure 5.7, when the PV voltage drops to zero due to the existence of the SCF in the IB MOSFETs, the converter enters the faulty state triggered by the proposed fault detection algorithm. The converter continues to run in the MPP even after a fault occurrence and subsequent topology reconfiguration. In addition, the OB is reconfigured into a half-bridge rectifier to recover the converter DC voltage gain range.


FB
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I_{PV}
V_{PV}
S_1 SCF
V_{Cr}
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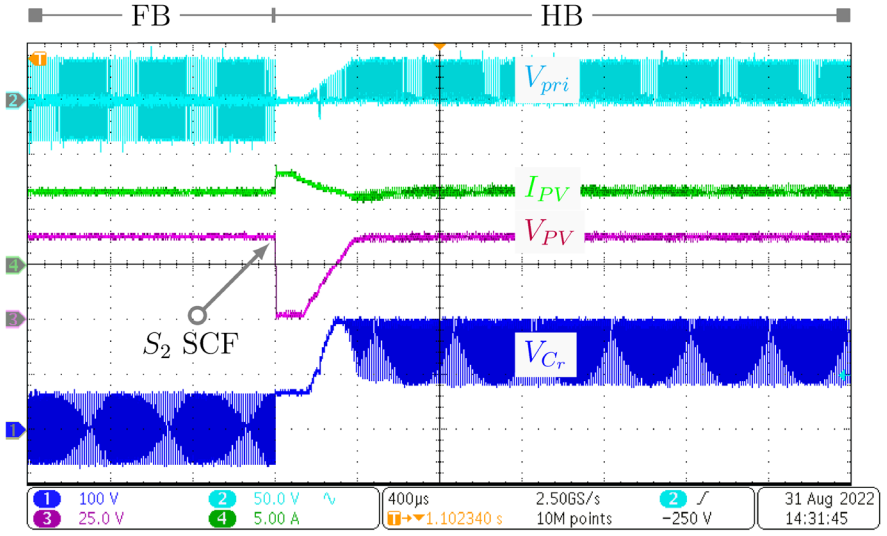
(a)


FB
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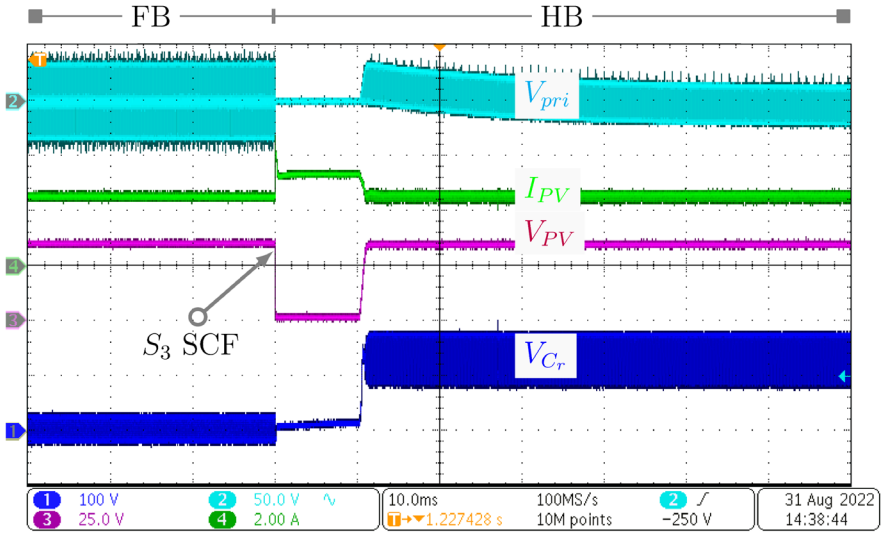
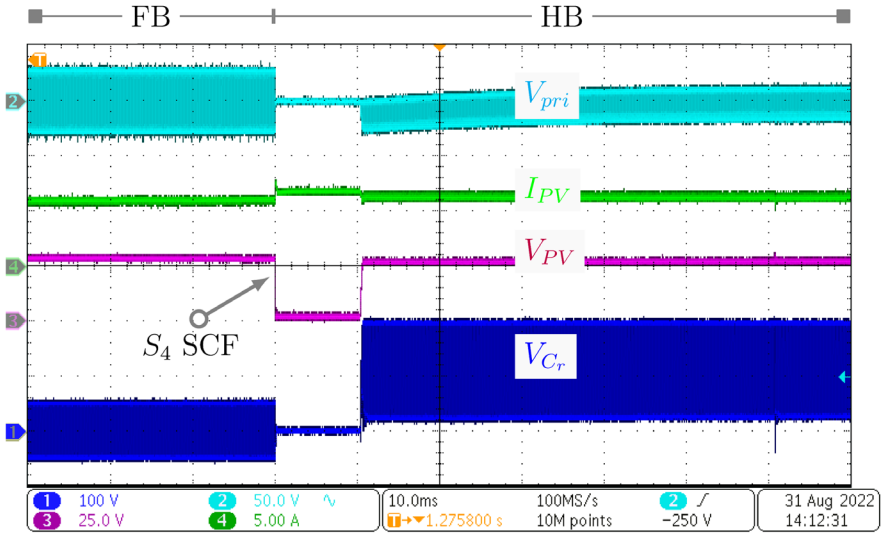


(c)



(d)

Figure 5.7 Experimental results for the SCF of input-side MOSFETs in different operating modes, locations, and operating power of the PV module: a) SCF in S_1 at the 65 W boost mode, b) SCF in S_2 in the 250 W buck mode, c) SCF in S_3 in the 90 W buck mode and d) SCF in S_4 in the 175 W boost mode.

When the output switch Q_2 experiences OCF, which is emulated using an external solid state relay, the PV current decreases, as shown in Figure 5.8, where subfigures (a) and (b) correspond to the buck and boost operation of the converter, respectively. This causes the OCF detection triggering. The OCF is detected within 80 µs, which is considered negligible for PV power loss. To remedy the OCF, the output switch Q_1 is activated in the same leg, as shown for the gate-source voltage signal of switch Q_1 ($V_{gs,Q1}$). This makes the resonant capacitor charge up to a DC bias of half the output voltage. The converter continues to extract the maximum power from the PV module after the OCF is remedied.

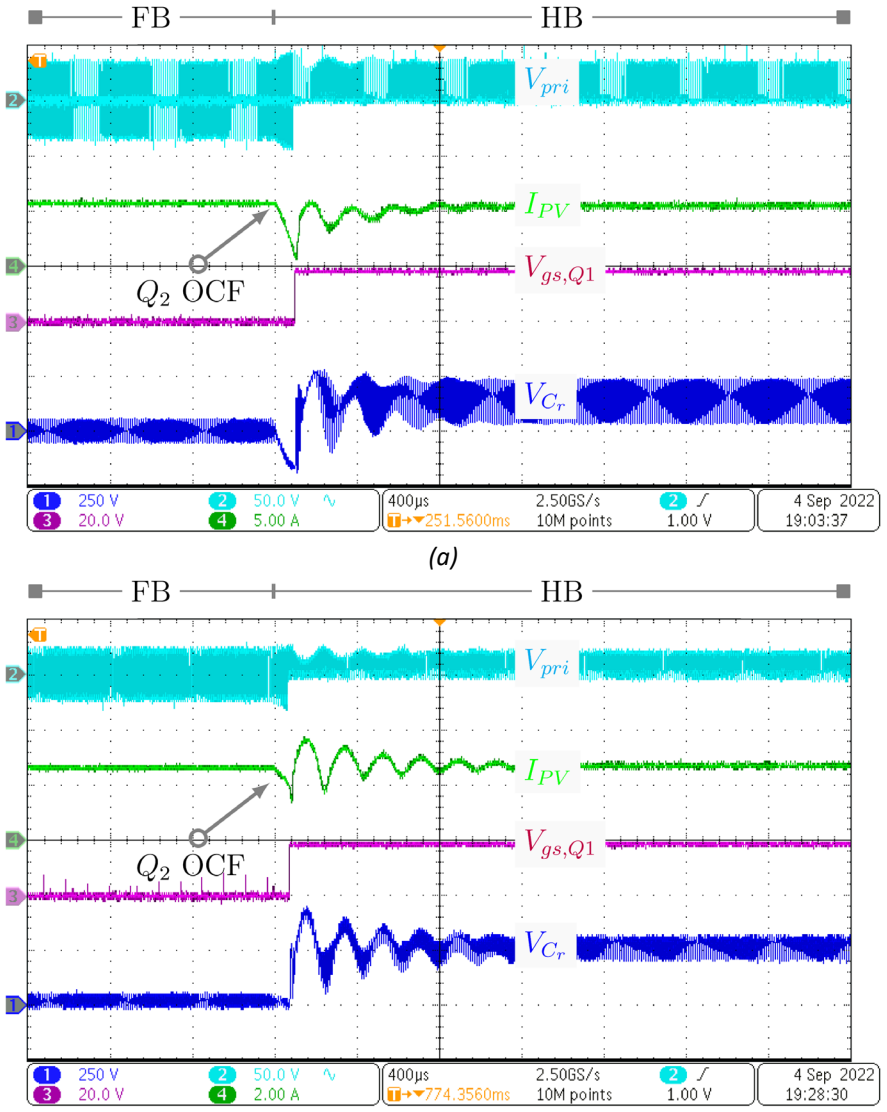


Figure 5.8 Experimental results for OCF output-side MOSFETs at a) buck mode 250 W and b) 65 W boost mode.

The experimental results for the SCF in Q_4 during buck and boost modes are shown in Figure 5.9, where subfigures (a) and (b) correspond to the buck and boost mode operation of the converter, respectively. The SCF was detected within 20 µs, i.e., less than two switching cycles. In this way, the converter was protected from further damage. Moreover, after the SCF, the switch Q_2 performs voltage boosting using the FHR modulation scheme, as shown in Figure 5.9b, in which $V_{gs,Q2}$ is the gate-source voltage of switch Q_2. After the fault remedy in both cases, the converter continues to harvest the maximum power from the PV module.

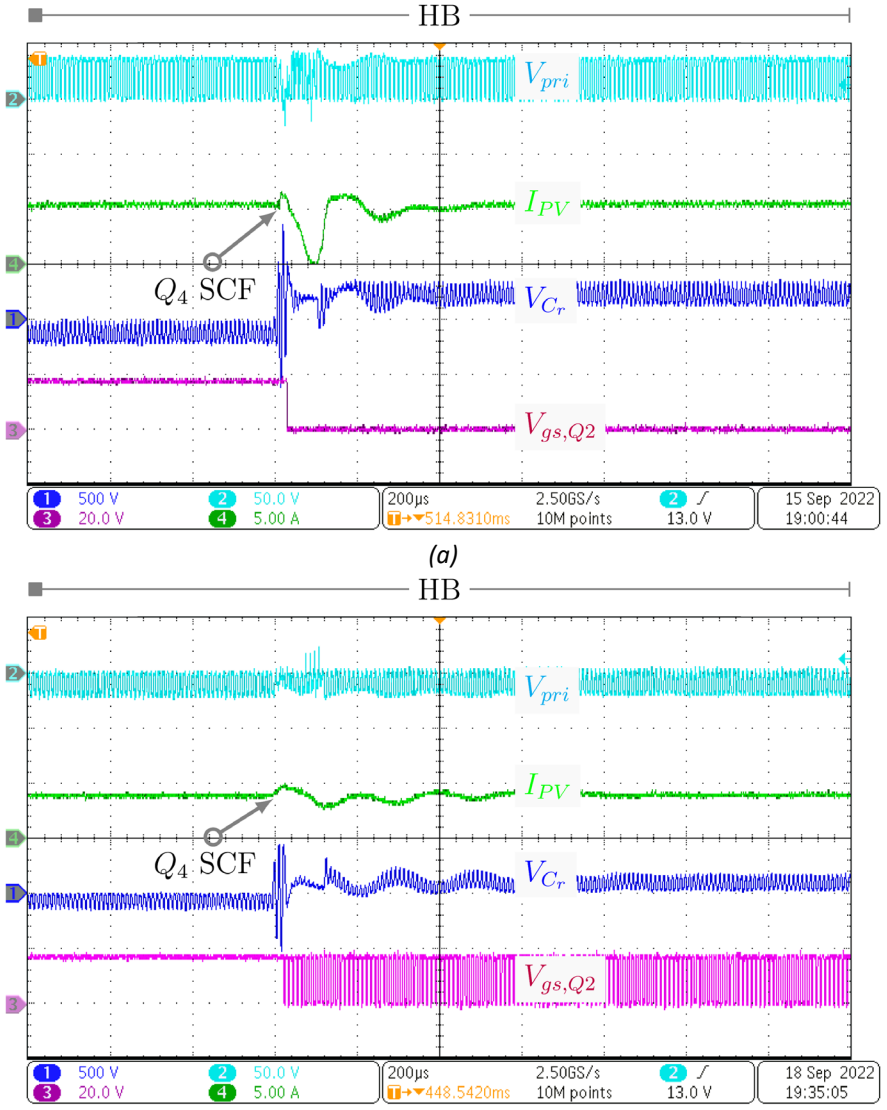


Figure 5.9 Experimental results for SCF output-side MOSFET S_4 at a) buck mode 200 W and b) 75 W boost mode.

The P-V and I-V characteristics of the PV module when operating at a derated power mode in buck and boost operation are validated experimentally, as shown in Figure 5.10. In both cases, the FT ZR-SRC is operating on the right from the MPP, which ensures greater efficiency.

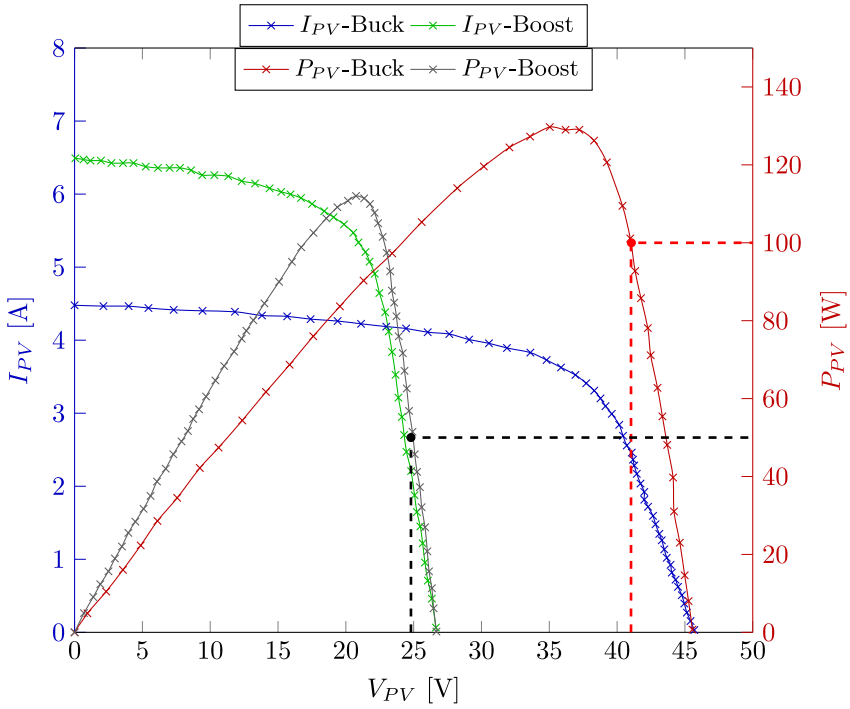


Figure 5.10 Experimental P-V curves for the ZR-SRC operation at derated power in the buck and boost modes.

5.5 Economic Assessment

The ZR-SRC is tested under the daily profile of residential PV applications in the normal and faulty state. The total energy of the PV module under the environmental condition considered with 100% MPPT efficiency is 1355 Wh. In a normal state, the total energy of the PV module is 1350 Wh, representing about 99.6% MPPT efficiency during the day. However, in the faulty condition with input power curtailed at 200 W, the cumulative PV energy drops to 1197 Wh. Therefore, this converter design with input power curtailment at 200 W will exhibit approximately the same pre- and post-fault failure rates, as demonstrated in [PAPER-VII]. Consequently, the difference between PV energy delivered in normal and faulty states is estimated to be around 150 Wh, considered the worst-case scenario when no cloud cover exists.

5.6 Summary

This chapter presented and verified experimentally fault identification and remedy methods for the proposed self-healing PV microconverter based on the FT ZR-SRC topology. The proposed technology provides fast SCF and OCF identification with acceptable speed, allowing converter cost minimization. Furthermore, the suggested fault detection system is implemented using an analog component to reduce the cost and computational constraints on the digital platform. The experimental findings validated the usefulness of the converter in many operating scenarios. In addition, they prove the validity of the fourth hypothesis.

The obtained results justify the feasibility and good practical value of FT ZR converters. The low implementation cost resulting from avoiding auxiliary semiconductor components enables the use of FT converters in cost-sensitive applications.

6 Conclusions and Future Work

The thesis proposed the concept of the fault-tolerant zero-redundancy DC-DC converter based on the SRC. The author proposed the fault-tolerant zero redundancy SRC-based isolated buck-boost DC-DC converter, contributing to the development and justification of the zero-redundancy fault tolerance converters. This converter is very practical as it has low implementation costs but requires some power curtailment when a fault occurs. A trade-off is demonstrated between increasing the size and cost of a converter in order to maintain performance before and after a failure versus having a zero-redundancy converter with an overloaded component after a fault. A converter of this type must be thermally engineered to withstand increased ohmic losses in short-circuited MOSFETs. Proper thermal design is important because high ohmic losses can cause the converter to heat up and fail catastrophically. This conclusion comes from the experimental verification of the post-fault characteristics of short-circuited MOSFETs performed by the author, which demonstrated increased resistance after a fault. This proves the feasibility of zero-redundancy fault-tolerant galvanically isolated DC-DC converters.

Furthermore, the extensive laboratory experiments indicate that using a defective switch as a current conducting path in a reconfigurable fault-tolerant DC-DC converter makes the zero-redundancy fault tolerance concept practical. The employed converter has high reliability due to its fault-tolerant capability, making it suitable for residential PV applications. Moreover, it has the self-healing capability to continue its operation even in a faulty state. This enables the converter to operate in the field without unplanned maintenance in the case of a random fault.

The author has established a methodology for the reliability assessment of galvanically isolated DC-DC converters before and after a fault. The reliability study based on the high-resolution PV mission profile indicates that the power semiconductors are considered the most fragile components in the converter, warranting careful consideration during the design phase of the converter. It is demonstrated by the author that the FIDES Guide provides established empirical models capable of accounting for the actual stress of the components in the PV microconverter, allowing the possibility of providing more accurate lifetime predictions. These findings are demonstrated using the proposed SRC-based zero-redundancy fault-tolerant isolated buck-boost DC-DC converter. The results support the fundamental hypothesis that the system's random failure rate is primarily caused by the primary-side semiconductors, with the output-side switches having little impact. Moreover, the analytical results obtained by the author demonstrate that the mission profile significantly influences the failure rate of the components of PV DC-DC interface microconverters and can lead to an overestimation of the converter's lifetime. It is worth mentioning that author found that the sampling time of the mission profile should be in the order of seconds in order to provide an accurate reliability estimation, which could be overestimated by up to two times if a low-resolution dataset is used.

The author has also developed a fault detection method for the primary semiconductor components, where the existing measurements used for MPPT are reused for input-side SCF detection. This enabled the design of the converter with low cost and minimized size. The author has confirmed the proposed fault detection and diagnosis strategies experimentally. The author found that the PV power must be curtailed after a fault to improve the reliability of the FT DC-DC converter with zero redundancy and, thus, extend its lifetime. The author has demonstrated how the power curtailment method must be

designed using the reliability analysis methodology he developed. Moreover, the author has created a measurement station recording solar irradiance and ambient temperature with high resolution in Tallinn. This dataset is released as open source and continuously updated to provide researchers and the public sector with more tools for analyzing photovoltaic power systems.

As the author identified, the transformer is the crucial component defining converter performance before and after a fault. However, its optimization for operation in a wide input voltage range is challenging. Hence, future work will concentrate on multi-objective optimization of the transformer design to achieve the balanced pre-and post-fault performance of the proposed converter.

In addition, future research should be directed towards extending the proposed methodology based on the FIDES Guide with an analysis of manufacturing uncertainties using the Monte Carlo method. Moreover, the methodology developed by the author should be updated considering the newest edition of the FIDES Guide, which is already published in French and scheduled to be published In English in 2023.

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Abstract

Fault-tolerant Galvanically Isolated DC-DC Converters with Zero Redundancy

This Ph.D. thesis introduces the fault-tolerant zero redundancy galvanically isolated DC-DC converter concept, which is demonstrated using the topology of the isolated series resonant DC-DC converter (FT ZR-SRC). The proposed buck-boost converter can regulate the input voltage in a wide range, making it suitable for residential photovoltaic (PV) systems. Furthermore, the proposed converter can handle faulty conditions on-the-fly using topology reconfiguration without auxiliary components. Despite the low number of components, the converter can withstand several semiconductor faults, which was not previously demonstrated for high step-up DC-DC converters.

The thesis investigates the MOSFET post-fault characteristics for operation in fault-tolerant DC-DC converters. The results prove the feasibility of the zero redundancy fault tolerance as the short-circuited switch can be used as a current conducting path in a reconfigurable fault-tolerant DC-DC converter. However, the thermal design should account for ohmic losses in a short-circuited MOSFET with post-fault resistance several times higher than the on-state resistance. In addition, a control system should implement a power curtailment algorithm limiting the stresses of remaining healthy components.

The reliability of the proposed FT ZR-SRC is evaluated using a high-resolution yearly mission profile of solar irradiance and ambient temperature and the methodology developed by the author. This thesis yields a 1-second resolution recorded by the author in Tallinn, Estonia. The proposed reliability analysis approach is based on the FIDES Guide, which considers the physics of the failure while calculating the random failure rate of the components. The FIDES Guide provides a more realistic lifetime prediction based on well-established empirical models linking the random failure rate and instantaneous component stress. The results indicate that the primary semiconductors and the transformer are the most vulnerable component in the FT ZR-SRC.

The design guidelines for the FT ZR-SRC are provided for PV applications. Also, low-cost diagnosis and detection methods were developed for ZR-SRC considering residential PV applications. The results demonstrate that the proposed converter can detect a fault accurately in 20 µs to 20 ms, depending on the fault type. Aside from high-speed and accurate detection, it provides on-the-fly reconfiguration with no efficiency deterioration after a fault, distinguishing it from similar solutions in the literature. Furthermore, no false positive detections were observed during extensive laboratory testing.

The thesis provides a design approach for power curtailment control that maintains the random failure rate of the ZR-SRC components constant before and after a fault while minimizing the loss of annual energy yield. Moreover, the developed power curtailment algorithm allows the converter to continue operation at nearly the same efficiency by avoiding high stress on the remaining healthy components.

This thesis has substantial practical value as the proposed concept could increase the availability of cost-sensitive applications in DC microgrids, such as residential PV. The knowledge of zero redundancy fault tolerance contributes to the field of galvanically isolated DC-DC converters. Furthermore, the developed technology is scalable, providing opportunities for more reliable power electronics in low-cost consumer applications and reducing implementation costs in mission-critical applications.

Lühikokkuvõte

Null-liiasusega veatolerantsed galvaanilise isolatsiooniga alalispingemuundurid

Doktoritöö käsitleb null-liiasusega veatolerantsete galvaanilise isolatsiooniga alalispingemuundurite kontspeti, mida uuriti isoleeritud jada-resonants pinget tõstva/madaldava alalispingemuunduri (FT ZR-SRC) näitel.

Väljapakutud FT ZR-SRC muundur suudab sisendpinget reguleerida laias vahemikus, muutes selle sobivaks eramute fotogalvaanilistele (PV) süsteemidele. Väljapakutud muundur tuleb vigadega toime tööd katkestamta, kasutades selleks topoloogia ümberkonfigureerimist ilma abikomponentideta. Vaatamata komponentide vähesele arvule suudab muundur taluda mitmeid pooljuhtide rikkeid, mida varem suure võimendusega alalispingemuundurites ei ole saavutatud.

Lõputöös uuritakse MOSFET-i rikkejärgseid karakteristikuid rakendamaks neid veatolerantsetes alalispingemuundurites. Tulemused tõestavad, et null-liiasusega on võimalik saavutada teatud veatolerantsus. Näiteks lühises transistori saab kasutada voolu juhtiva rajana ümberkonfigureeritavas alalispingemuunduris. Soojuslik analüüs näitas, et sealjuurs tuleb arvestada suuremate juhtivuskadudega kuna lühises MOSFETi rikkejärgne takistus on mitu korda suurem kui takistus normaalrežiimis. Samuti peab juhtimissüsteem piirama võimsust selleks, et vältida tervete komponentide ülekoormust.

Väljapakutud muunduri FT ZR-SRC töökindlust hinnati kõrge resolutsiooniga iga-aastase päikesekiirguse ja ümbritseva õhu temperatuuri profiili ja autori poolt välja töötatud metoodika abil. See lõputöö annab 1-sekundilise eraldusvõime, mille autor on salvestanud Tallinnas, Eestis. Välja pakutud töökindluse analüüsimeetod põhineb FIDES-i juhendil, mis võtab komponentide juhusliku rikkemäära arvutamisel arvesse rikke füüsikat. FIDES-i juhend pakub realistlikut eluea prognoosi, mis põhineb väljakujunenud empiirilistel mudelitel. Tulemused näitasid, et primaarsedpooljuhid ja trafo on FT ZR-SRC kõige haavatavamad komponendid.

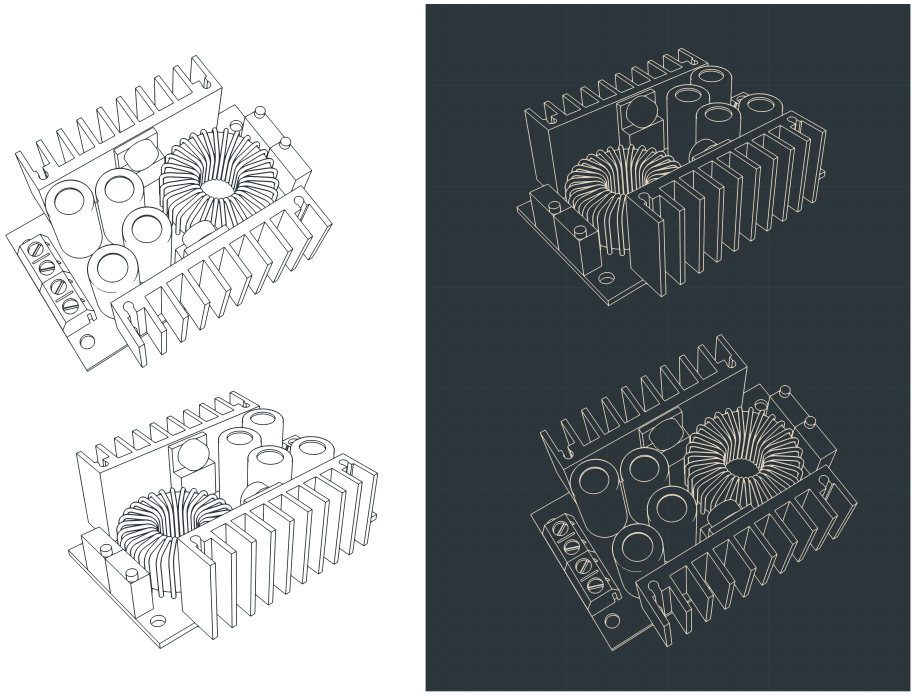
FT ZR-SRC projekteerimisjuhised on ette nähtud fotoelektriliste rakenduste jaoks. Lisaks töötati ZR-SRC jaoks välja odavad diagnoosi- ja tuvastamismeetodid, võttes arvesse PV rakendusi. Kavandatav muundur suudab olenevalt vea tüübist tuvastada vea täpsusega 20 µs kuni 20 ms jooksul. Lisaks kiirele ja täpsele vea tuvastamisele pakub muundur veajärgset ümberseadistamist ilma, et töö katkeks või energiatõhusus väheneks. See on omadus, mis eristab seda kirjanduses leiduvatest teistest lahendustest. Ulatuslike laborikatsete käigus ei tuvastatud ühtegi valepositiivset tulemust.

Lõputöö pakub välja konstruktsioonilahenduse veajärgseks võimsuse piiramiseks, mis hoiab ZR-SRC komponentide juhusliku rikkemäära konstantsena nii enne kui ka pärast riket. Samal ajal minimeeritakse aastast energiatootluse kadu. Samuti võimaldab väljatöötatud võimsuse piiramise algoritm muunduril jätkata tööd peaaegu sama efektiivsusega, vältides ülejäänud tervete komponentide ülekoormamist.

Sellel doktoritööl on oluline praktiline väärtus, kuna väljapakutud kontseptsioon võib suurendada kulutundlike rakenduste kättesaadavust alalisvoolu mikrovõrkudes. Teadmised null-liiasusega saavutatud tõrketaluvuse kohta aitavad kaasa galvaaniliselt isoleeritud alalispingemuundurite arengule. Väljatöötatud tehnoloogia on skaleeritav, pakkudes võimalusi töökindlamaks jõuelektroonikaks odavates tarbijarakendustes ja vähendades juurutuskulusid missioonikriitilistes rakendustes.

Appendix

[PAPER-I] **A. Bakeer**, A. Chub, and D. Vinnikov, “Full-Bridge Fault-Tolerant Isolated DC-DC Converters: Overview of Technologies and Application Challenges,” in IEEE Power Electronics Magazine, vol. 9, no. 3, pp. 45–55, Sept. 2022, doi: 10.1109/MPEL.2022.3196565.



Full-Bridge Fault-Tolerant Isolated DC–DC Converters: Overview of Technologies and Application Challenges

by Abualkasim Bakeer, Andrii Chub, and Dmitri Vinnikov

Nowadays, energy generation is on the path from centralized to distributed generation paradigm to improve the efficiency and resilience of power systems. One of the major developments in the energy sector was the introduction of dc microgrids that facilitate direct integration of energy sources, storage, and dc loads. Also, most consumer and industrial devices are naturally dc devices or contain a dc link, which makes them compatible with dc microgrids. Hence, dc distribution is an efficient tool for combining dc energy sources and battery energy storage with typical loads that are predominantly compatible with dc microgrids. In the foreseeable future, widespread adoption

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of dc microgrids will rely on the ubiquitous use of dc–dc converters. Apart from cost concerns, the long-term reliability of power electronic systems is under scrutiny by the power industry, which prefers simple but highly reliable/available solutions.

Among isolated dc–dc converter topologies, flyback and forward converters are used the most in low-power applications. These topologies are simple and, thus, cost-efficient, but they do not allow for fault-tolerance implementation. They could be overdesigned for higher reliability, but their cost would render their adoption unfeasible. Conventional (N + 1) redundancy could be used in a limited number of mission-critical systems where the cost of implementation is a secondary issue. However, the cost of implementation and maintenance still play an essential role in most applications. Therefore, fault-tolerant (FT) dc–dc converters are becoming increasingly popular as a tool enabling a deferred after-fault maintenance of mission-critical systems [1].

In the foreseeable future, widespread adoption of dc microgrids will rely on the ubiquitous use of dc–dc converters.

The literature on the isolated fault-tolerant dc–dc converters presents full-bridge topologies primarily due to their control versatility offering various switching patterns. They are capable of on-the-fly topology morphing into equivalent topologies with a reduced number of switches, like half-bridge, flyback, or single-switch [2]–[5], providing ample opportunities for a semiconductor fault remedy. Component-level fault tolerance is also possible, but could be costly due to the high number of extra components [6]. Scaling up the typical dc–dc converters to the medium and high power levels typically requires a parallel connection of several dc–dc converter cells, which suggests (N + 1) redundancy for fault tolerance implementation. Operation with medium to high voltages requires the implementation of multi-switch topologies to match blocking voltage requirements [7], which enables component-level fault tolerance by adding a few extra submodules or series switches [8], [9]. Moreover, fault tolerance could be implemented at the level of each submodule [10].

This article discusses the implementation possibilities of full-bridge fault-tolerant galvanically isolated dc–dc converters and their practical limitations. The known approaches are categorized into two groups: those with redundant components and with zero redundancy (Table 1). Both types can operate after a semiconductor fault until the next scheduled maintenance. The main implementation principles are demonstrated using series resonant dc–dc converter (SRC) topology as it was used the most in the literature. Moreover, some phase-shifted topologies, like the dual active bridge, are not feasible in implementation with zero redundancy and thus cannot be used as a case study [11]. Only semiconductor faults are considered as they were reported to be the most frequent in isolated dc–dc converters [12]. Fault detection techniques are

Table 1. Comparison between different FT approaches for full-bridge galvanically isolated dc–dc converters.

Item	Redundant active leg [16]	Redundant capacitors leg [20], [21]	Zero redundancy [22]–[24]
Example	Figure 1(a)	Figure 1(b)	Figures 2(a) and (c) and 3(a)
IB/OB switch type	IGBT	MOSFET/IGBT	MOSFET/IGBT
Reported power range	> 350 W	> 350 W	< 350 W
Post-fault overloading of components	No	Yes	Yes
Power curtailment	Not Needed	Needed	Needed
Extra components	■ 4 Aux. switches ■ 4 Semiconductors ■ 12 Fuses	■ 4 Aux. switches ■ 0 Semiconductors ■ 0 Fuses	■ 0 Aux. switches ■ 0 Semiconductors ■ 0 Fuses
Power density	XXX	XX	X
Cost	$$$	$$	$
Reported applications	■ UPS ■ Data Center	■ UPS ■ Data Center	■ Residential PV ■ Battery charger ■ Light-emitting diodes

X is the smallest design, XXX is the biggest design.
$ is the cheapest, $$$ is the most expensive.

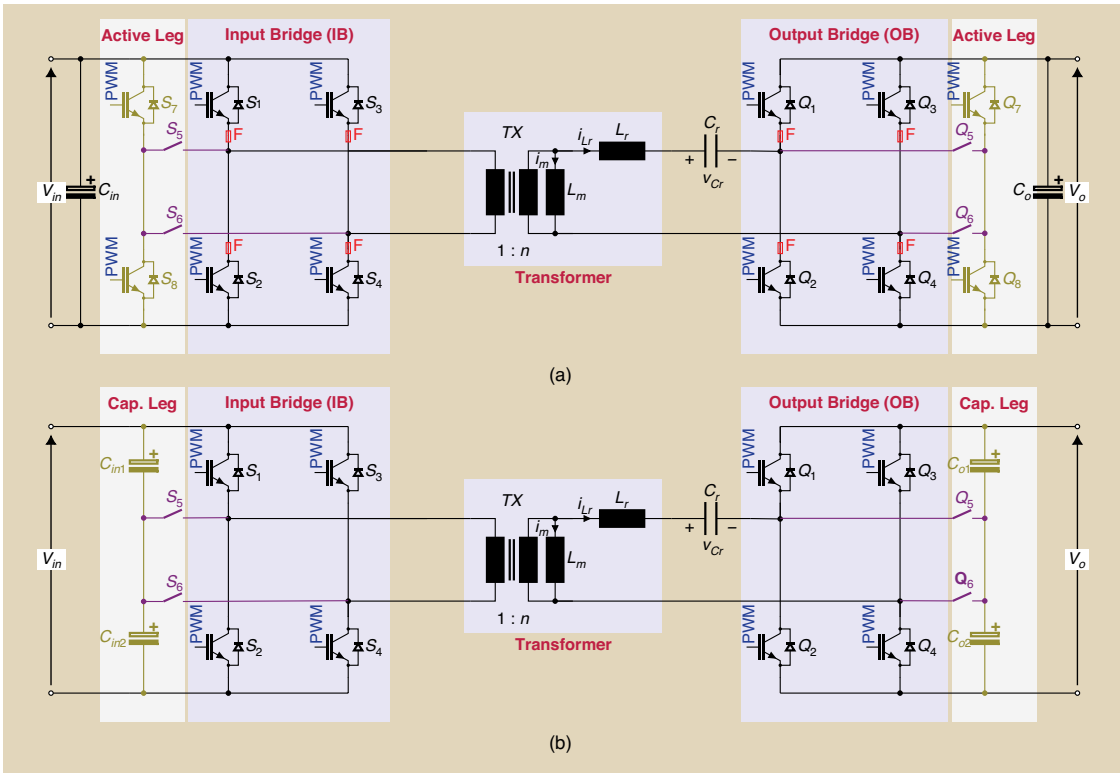

FIG 1 A fault-tolerant isolated dc–dc converter using redundant components on the input and output sides. (a) FT SRC with a redundant active leg [16]. (b) FT SRC with a redundant capacitors leg with midpoint connection [20], [21].

not presented as they have been reviewed and categorized in [9], [13], and [14].

The article overviews three main approaches to the realization of the fault tolerance to semiconductor faults in full-bridge galvanically isolated dc–dc converters. It demonstrates a trade-off between using extra components or reducing converter operating power after a fault to avoid overheating healthy components or penalizing the converter efficiency after a fault.

Fault-Tolerant Converters With Redundant Components

Using redundant components to overcome converter failure conditions is the most common way to prevent power outages in mission-critical applications [1], extending converter useful life and availability. This refers to redundancy at the component level within a single converter using additional hardware, like semiconductors, capacitors, auxiliary switches, and fuses to isolate the faulty component, as shown in Figure 1. Isolated dc–dc converters suffer the most from semiconductor faults, as the statistics report that input-side semiconductors are the most vulnerable components [12]. In general, the converter semiconductors have two typical fault states depending on the failure mechanism: an open-circuit fault (OCF) and short-circuit fault (SCF) [15]. After fault detection and identification, an FT converter can be revived by the control system. The auxiliary switches (i.e., $S_{5,6}$ and $Q_{5,6}$) operate in an on/off mode and can be implemented as an electromechanical relay, a static solid-state relay (SSR), or using two MOSFETs connected in the back-to-back configuration. This group of FT approaches is tolerant to both the OCF and the SCF in the input/output bridge (IB/OB) semiconductors. The auxiliary switch connects unused redundant components depending on the fault location on either the input or output side.

The known approaches are categorized into two groups: those with redundant components and with zero redundancy.

The first FT approach (Figure 1a) uses redundant switching legs (i.e., active legs) on the input and output

sides. It requires a fuse (designated as "F" in Figure 1a) in series with each semiconductor in the converter to isolate an SCF and transform it into an OCF after thermal fuse breakdown [16]. By following this way, to achieve complete isolation of the faulty leg from the converter operation, the healthy switch in the faulty leg should be turned off continuously. One of the drawbacks of using the fuses is that they dissipate power losses during normal operation and thus affect the converter efficiency [12]. In addition, the presence of the fuse will increase parasitic inductance in the power circuit [16]. Moreover, the redundant leg in the FT converter compromises the converter cost as redundant switches require extra gate drives and auxiliary power supply circuitry.

On the other hand, with this FT approach, the converter components can handle the same power before and after the fault occurrence without overloading the components. The switches of the redundant leg are dimensioned or selected in the same way as for the main inverter legs. This FT approach is limited to implementations with IGBTs, as these transistors can survive relatively long overcurrent intervals before the fuse burns.

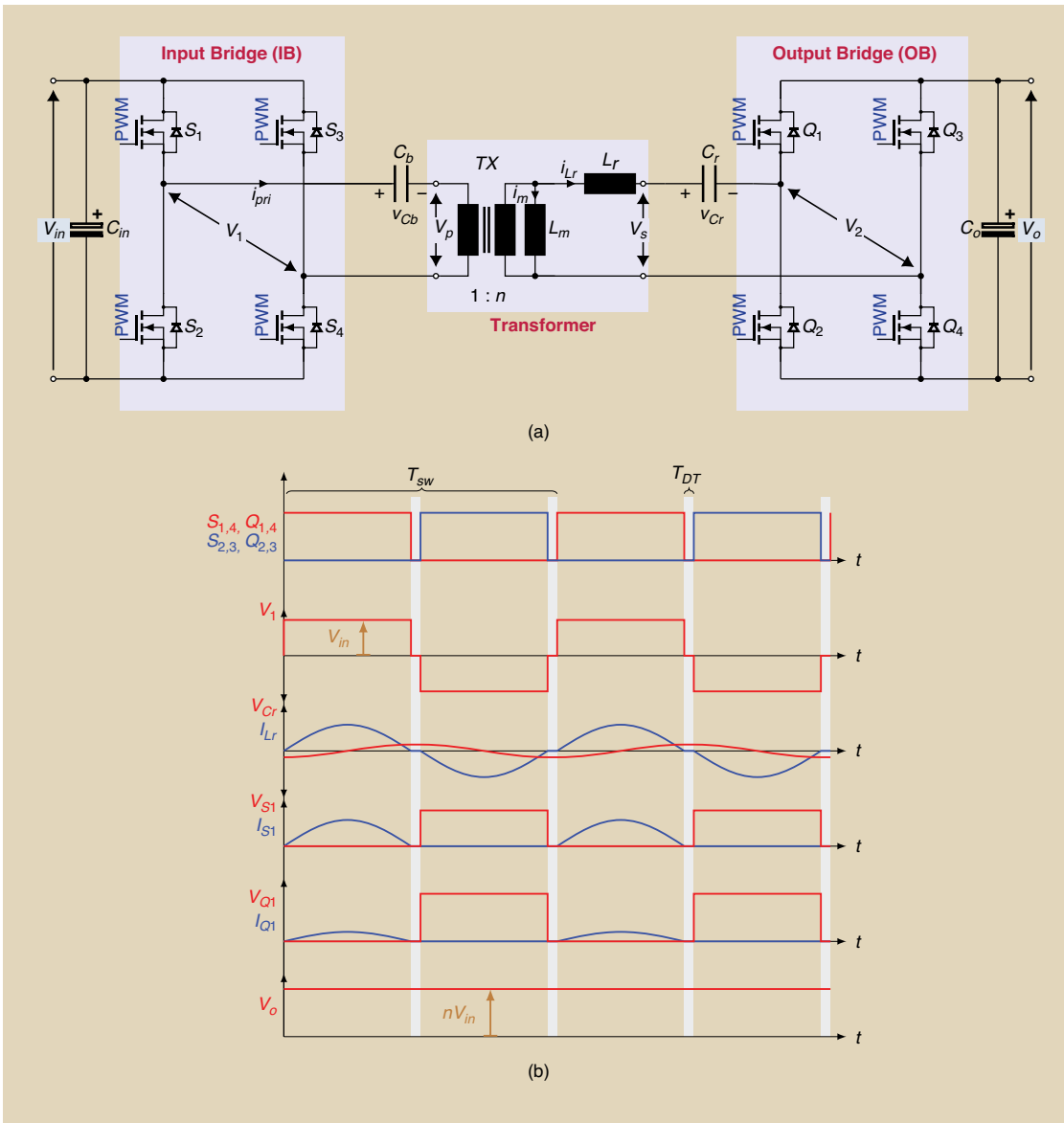

FIG 2 The FT SRC with a zero redundancy and TMC-based post-fault control [22]. (a) Main circuit. (b) Idealized steady-state waveforms during normal operation.

MOSFETs do not show the same overloading ruggedness and are likely to burn before the fault is identified and a fuse disconnects the corresponding power device. For example, many IGBTs today can withstand the short-circuit current for up to 10 μs, thus allowing for sufficient time for fault detection and identification (which could require less than one switching period) and burning of a fuse caused by the short-circuit current [17].

The low-voltage Si MOSFETs are most likely to experience SCF with post-fault ON-state resistance up to an order of magnitude higher than the datasheet value, which should be taken into account during the thermal design of a fault-tolerant converter [18]. SiC devices used in high voltage ports of dc–dc converter shown roughly 80%/20% distribution between SCF and OCF [18]. It was also shown that some devices could fail to conditions between SCF and OCF, but those cases will eventually converge to either SCF or OCF due to excessive power dissipation in a faulty device [19].

The second FT approach has a redundant capacitors leg with a midpoint on the input and output sides, as shown in Figure 1b [20], [21]. It requires four bidirectional

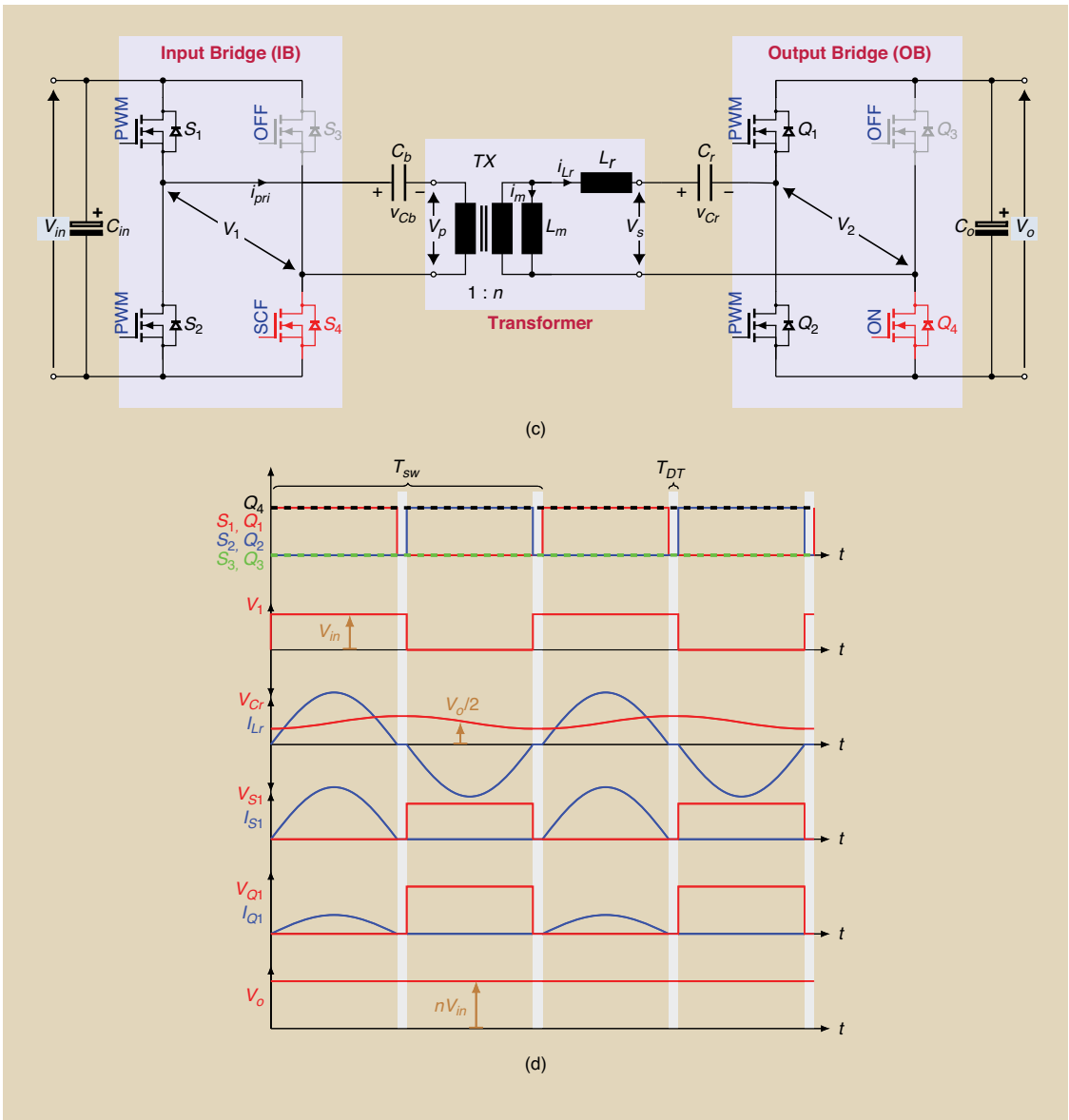

FIG 2 (c) Example of a possible reconfiguration after the fault in the MOSFET switch S1. (d) Idealized steady-state waveforms during post-fault operation.

auxiliary switches (up to eight discrete switches in solid-state implementation) to connect a faulty leg to the corresponding midpoint. Unlike the previous FT approach, IB/OB could be realized using IGBT or MOSFET devices, and the fuses are no longer required. However, only OCF could be remedied in the bridge that does not have a capacitor in series with the transformer winding. The key to this FT approach is to keep the converter running after a failure, but as a half-bridge instead of a full-bridge on the faulty side. Similarly, the healthy side should be reconfigured into a half-bridge inverter or rectifier operating synchronously with the other side. After such a reconfiguration, the average voltage across the resonance capacitor C_r is increased to half of the output voltage. The auxiliary switches are used to reconfigure a healthy converter side, IB or OB, to ensure post-fault operation of the FT SRC with the same dc gain as before the fault. In the case of SCF, the damaged switch is used as a conduction path for the current, while another switch on the same leg is turned off, e.g., S_3 should stay open if S_4 causes SCF. The reconfiguration of the healthy bridge into a half-bridge is functionally similar to commutating auxiliary transformer winding to adjust the total converter gain [22], which could be disadvantageous in practice due to the oversized design of the transformer. Since the power supplied by the dc–dc converter is constant before and after the fault, the remaining healthy components could be overstressed.

The key to this FT approach is to keep the converter running after a failure, but as a half-bridge instead of a full-bridge on the faulty side.

Fault-Tolerant Converters With Zero Redundancy

The zero redundancy FT SRC shown in Figure 2a was first proposed in [23]. Its basic idea originates from the assumption that the conventional SRC can utilize a short-circuited transistor or continuously turned-on transistor as a current conducting path, eliminating auxiliary switches and associated circuitry. Moreover, having only active transistors, this converter can operate as an isolated buck–boost converter (IBBC) by applying special modulations to IB and OB.

This FT approach is based on the topology morphing control (TMC) that enables self-sufficient post-fault converter operation without additional components in the primary circuit. The FT SRC implementing the TMC contains only two hybrid switching bridges at the input and output, which can be reconfigured as a full- to a half-bridge after the fault is detected. The blocking capacitor C_b ensures the dc bias in the transformer current is eliminated, avoiding saturation of the transformer core after reconfiguration. Additionally, C_b could have a high capacitance not to affect the IBBC resonant frequency. The idealized steady-state waveforms of the IBBC during the normal (healthy) state are depicted in Figure 2b, where the IBBC is operating as a typical full-bridge SRC. The IB feeds the transformer with balanced rectangular voltage pulses, while the OB operates as a synchronous rectifier. Its post-fault operation in buck and boost modes is based on application of asymmetrical modulations as presented in [11].

The considered zero redundancy FT SRC can withstand a single fault (either OCF or SCF) in IB and OB semiconductors, i.e., up to two semiconductor faults when they happen on the different sides of the converter. Each faulty inverter bridge can be easily reconfigured into a half-bridge in the case of a semiconductor fault, as shown in Figure 2c for the IB. During the post-fault operation, the average voltage across C_r equals half of the output voltage (Figure 2d). Similarly, the blocking capacitor C_b operates at increased voltage stress of half the input voltage, assuming that $C_b \gg C_r \cdot n^2$.

Consequently, the total gain of the converter remains the same before and after a semiconductor fault. This FT approach is compatible with both MOSFETs and IGBTs. The output voltage of the zero redundancy FT SRC remains constant after a fault, but the RMS current stresses of the transformer and the semiconductor devices are increased to twice the RMS current in the normal state at the same load, increasing the thermal loading of the converter components. This FT approach does not require an additional fuse in series with each semiconductor. A shorted semiconductor is used as a current path in the circuit. For any fault type (OCF/SCF) in the IB of the example FT SRC, the healthy OB must be reconfigured from the full-bridge into an asymmetrical (Greinacher) voltage doubler rectifier using one of the four possible implementations [22]. This FT approach has a thermal loading similar to that in the FT approach employing redundant capacitor legs with midpoint connections but at a much lower cost of implementation.

The comparison between the three presented FT approaches based on SRC topology is summarized in Table 1. It can be noted that there is a trade-off between adding extra components during the converter design, increasing the converter size and cost to maintain the same performance after a fault, and having zero redundant components, resulting in possible thermal overloads after a fault if power curtailment control is not utilized. The significantly increased thermal loading after a fault can also be observed for the FT approach with redundant capacitors legs with midpoint connections despite the use of extra components. Hence, out of these FT approaches, the one with zero redundancy can achieve better efficiency at a lower cost. It is worth mentioning that fault tolerance with zero redundancy and the redundant

capacitors leg both feature reduced voltage swing applied to the isolation transformer. As a result, those techniques are not practical in the dual active bridge-based converters, where the power delivery capacity of the converter depends directly on the transformer voltage swing [11].

Application Example of Zero Redundancy Fault-Tolerant DC–DC Converter

Owing to low realization cost, the zero-redundancy fault-tolerant approach has already found its application in PV microconverters [24]. PV microconverters are typically mounted on the same rail as the PV module it is connected to. Therefore thermal cycling and exposure to humidity require these devices to be protected according to a high-grade ingress protection code, like IP67 defined in IEC 60529. This makes the converter capable of withstanding snow, rain, wind, etc. Thermally conductive and water-resistant epoxy resins with moderate viscosity and low hardness are typically used for potting the converter enclosures. Recent industry trends show that conformal coating is a preferred solution to reduce converter weight, cost, and shipping fees. On the other hand, this packaging technology renders any repair unfeasible due to complicated and time-consuming disassembly, as shown from the example of the potted PV microconverter presented in Figure 3(a). Typically, faulty unit is replaced with a new one based on a valid warranty or under the terms of a service contract.

Nevertheless, getting a replacement could take a long time or incur extra-cost for unscheduled maintenance, which results in economic loss due to equipment downtime. The zero redundancy FT approach based on the TMC can reduce the downtime time to zero, making the PV microconverter operational till the next scheduled maintenance—a great advantage for residential PV installations regardless of possible performance deterioration after a fault. Figure 3b shows the power circuit topology of a zero redundancy FT PV microconverter [24]. It is based on the quasi-Z-source series resonant IBBC where

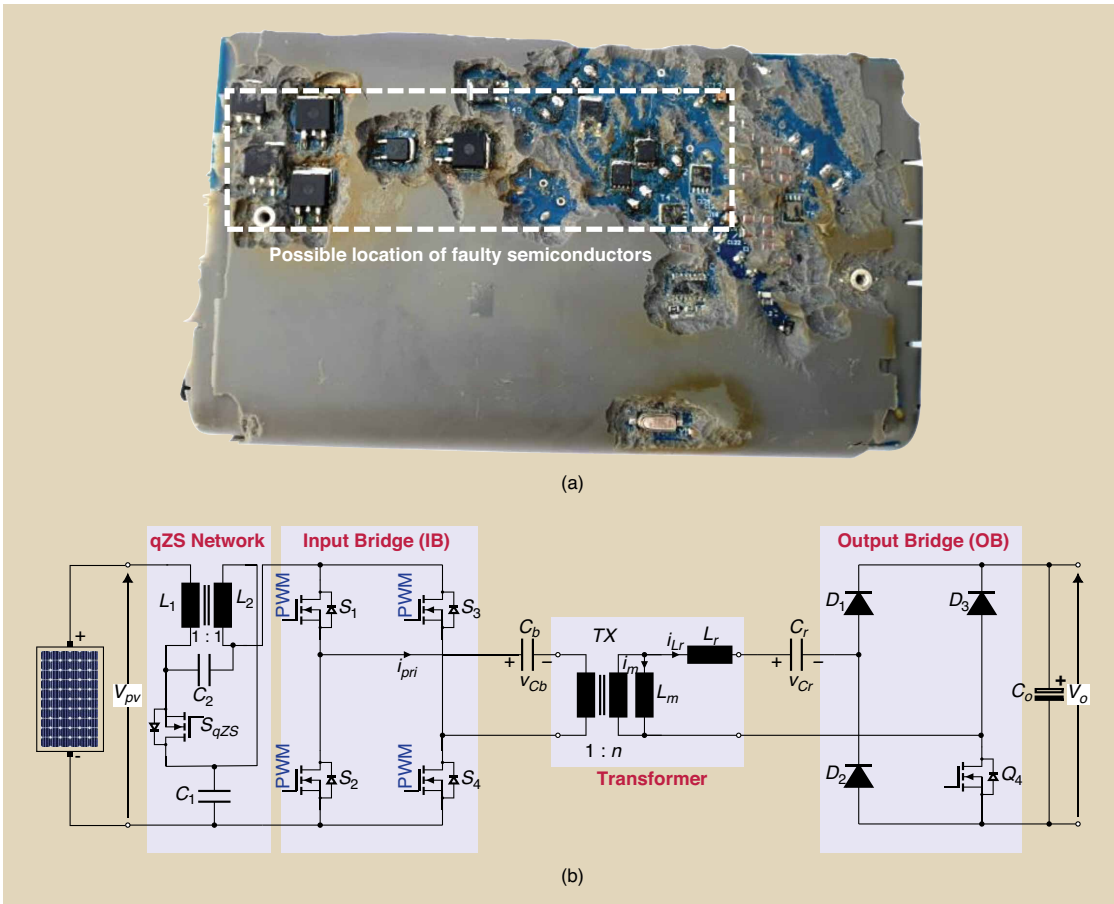

FIG 3 (a) Photo of the disassembled industrial PV microconverter with mechanically removed aluminum case and part of the potting compound. (b) Power circuit diagram of the zero redundancy fault-tolerant PV microconverter.

one of the rectifier diodes is replaced with the MOSFET to enable the TMC implementation.

Throughout its prognosed lifetime, the microconverter normally operates as a full-bridge quasi-Z-source SRC with the full-bridge rectifier. If the fault occurs in one of the input-side inverter switches, the microconverter is reconfigured into a single-switch quasi-Z-source converter. The topology morphing scenario depends on the operating point and is realized by applying one of the post-fault modulation sequences [24]. Figure 4 shows the performance benchmarking of the microconverter coupled with the 96-cell Silicon PV module before and after the short-circuit fault of a switch S_1. In both cases, the PV microconverter extracted total energy of 1190 Wh and showed the same average maximum power point (MPP) tracking efficiency of more than 99%. However, the power stage efficiency differs considerably for the pre- and post-fault operation. Before a fault, it achieves maximum efficiency of 95% at the maximum input power, as shown in Figure 4a, which results in the total

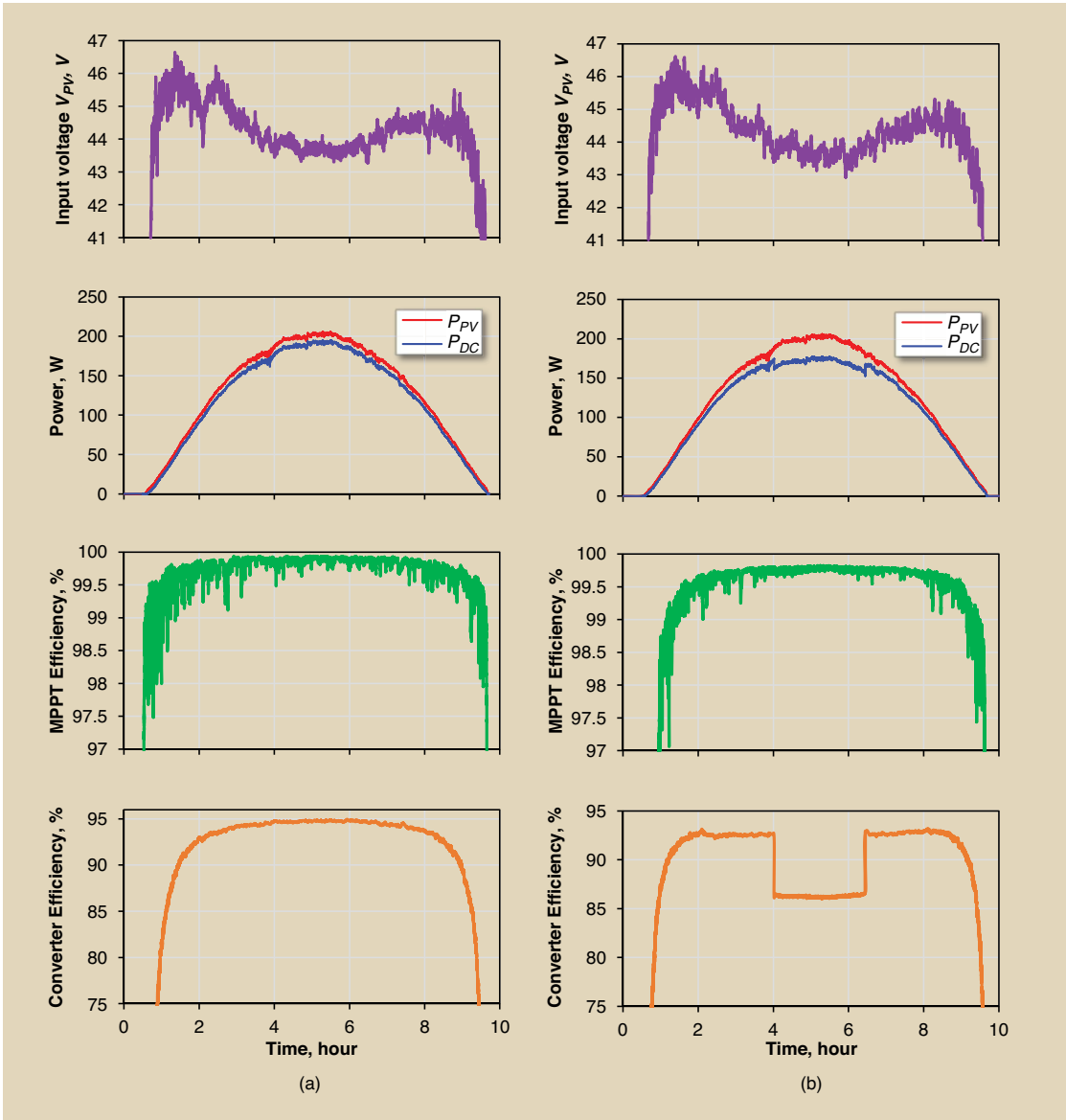

FIG 4 Experimental benchmarking of the zero-redundancy fault-tolerant PV microconverter coupled with 96-cell PV module using a clear day mission profile in (a) normal operation and (b) post-fault operation.

energy delivered to the output of 1116 Wh during a day (94% from the extracted PV energy). After a fault, the performance of the microconverter depends more strictly on the input voltage and, consequently, on the operating mode. It features relatively high efficiency in the buck mode at the input voltages above 44 V, which corresponds to the operation during the morning and evening hours, as could be seen from Figure 4b. During the peak solar irradiance hours, the MPP voltage of the PV module drops below 44 V, and the microconverter starts operating in a boost mode. In that case, the topology is reconfigured into the quasi Z-source (qZS) single-switch converter that suffers from relatively high current stresses. This results in an efficiency drop of 5%–6% and, consequently, daily output energy yield dropped down to 1070 Wh after a fault, which is 90% of the harvested PV energy. This is an acceptable performance deterioration considering that the converter can continue operating after a semiconductor switch fault.

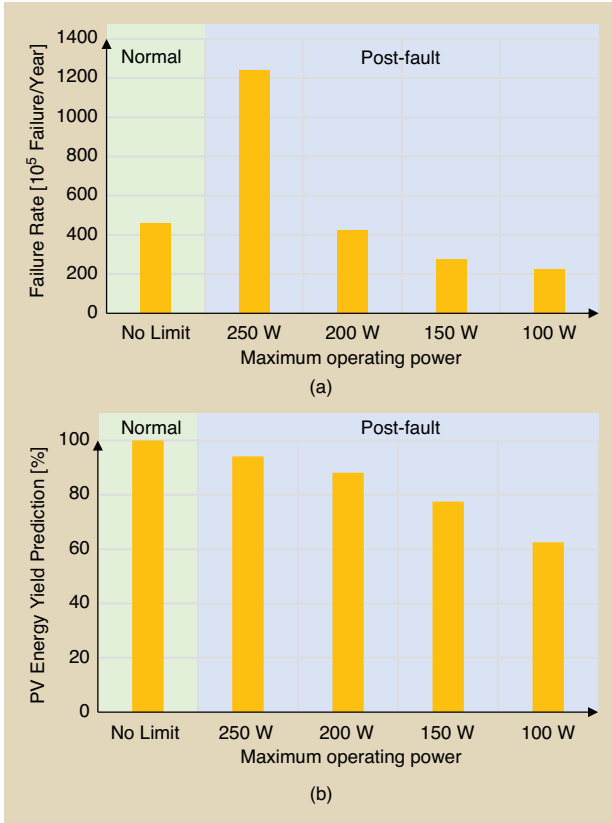

FIG 5 Reliability of the FT PV microconverter before and after the occurrence of a fault with power curtailment, considering the 60-cell Si residential PV module on the input side coupled with a dc microgrid of 350 V on the output side. (a) Yearly failure rate. (b) Yearly PV energy yield predictions.

Post-Fault Operation Issues of Zero-Redundancy Fault-Tolerant Converters

The efficiency of the zero redundancy FT dc–dc converters typically deteriorates after a fault, and the efficiency drop could vary significantly between the converter operation modes. This observation imposes an issue related to overloading of the critical components when attempting to operate close to the rated power after the fault-induced topology reconfiguration. If the zero redundancy FT converter continues delivering the rated power after the fault, the lifespan of the healthy components could be shortened as they will face high thermal stress or even catastrophic failure, depending on design trade-offs. For example, the low-cost designs use smaller printed circuit boards and cheaper semiconductors to meet the cost constraints. Hence the low-cost implementations of zero redundancy FT dc–dc converters may require software constraint (curtailment) of the input power to be introduced in the control system to ensure safe post-fault operation. On the other hand, in many applications, including PV, operation at the maximum power happens rarely and contributes only a small fraction of the annual energy yield [29].

A simple solution to improve the reliability of FT dc–dc converter with zero redundancy and, thus, extend its lifetime, is to curtail the converter input power at a certain level during infrequent PV energy production peaks. In the power curtailment mode, the failure rates of the critical components will be reduced significantly due to reduced thermal loading [25]. When the maximum power of the PV module becomes higher than the predetermined curtailment power level, the converter control system switches from the MPP tracking to the power derating mode. However, the microconverter input voltage will be different from the MPP voltage.

A trade-off between extending the converter reliability using power curtailment and associated reduction in the energy yield of the PV system should be considered. There are two possible solutions to the power curtailment problem: operating above and below the MPP voltage. In practice, the power curtailment to the point above the MPP voltage is more beneficial as high step-up converters tend to provide higher efficiency at lower dc gain [26], [27]. In addition, it is simpler to reach that point when starting MPP tracking from the open-circuit voltage of the PV module.

To define the random failure rate of the converter during its prognosed lifetime, the reliability approach from the FIDES handbook can be adopted [28]. This methodology allows for defining how the random failure rate of components operating under dc stress depends on the variations in component stress resulting from the

real-life yearly mission profile. The reliability was evaluated under a yearly mission profile of solar irradiance and ambient temperature adopted from Aalborg, Denmark [29]. Figure 5a shows the predicted random failure rate for the considered FT PV microconverter. In the pre-fault conditions, the PV microconverter experiences a moderate failure rate. After a fault appears, the control system curtails the maximum input power. Preliminary calculations showed that this PV microconverter would experience new faults next time it attempts to process the rated power of 300 W. If the input power is curtailed at the level of 250 W, the converter can continue operation after the topology reconfiguration but with much increased yearly random failure rate. The curtailment level should be reduced to 200 W to retain the random failure rate of a healthy microconverter. A further reduction of the curtailment level to 150 and 100 W shows a further reduction in the failure rate.

The main obstacle in designing zero redundancy systems is in achieving a trade-off between the cost of the converter and the level of post-fault power curtailment.

On the other hand, the PV microconverter with a low curtailment level cannot efficiently utilize the available PV energy, as predicted in Figure 5b. A healthy FT PV microinverter is predicted to deliver total energy of 309 kWh/year at the output terminals during the normal operation before the fault occurrence. The case of no power curtailment during the post-fault operation is avoided in Figure 5 as these conditions lead to a guaranteed catastrophic failure anytime the PV microconverter attempts to process powers close to the rated power. When the maximum operating power of 250 W is used, the PV microconverter loses only 9% of its energy yield estimated for the output side of the converter. Hence, it can continue its operation without catastrophic failures. For the power curtailment level of 100 W, the PV microconverter can still provide a little over 60% of the initial energy yield. It is worth mentioning that the dependence between the curtailment power level and energy yield loss would be much more substantial in southern climates, where more energy is produced at higher power levels compared to the reference case from Northern Europe.

Conclusions and Discussion

The article has discussed three FT approaches to overcoming semiconductor faults in galvanically isolated dc–dc converters using SRC as the reference topology. Among them, the zero redundancy FT approach shows the lowest implementation cost but requires some degree of power curtailment after a fault. This approach is based on the topology morphing control principle that allows converter topology reconfiguration using healthy switches and the shorted faulty switch as a current path in the post-fault topology.

As a result, post-fault maintenance can be delayed at no extra cost compared to the other two FT approaches. The most reasonable approach could be keeping the maintenance schedule after a fault occurred and was remedied to avoid costly urgent maintenance events. This helps avoid power outages and allows for a faster return on investment. The main obstacle in designing zero redundancy systems is in achieving a trade-off between the cost of the converter and the level of post-fault power curtailment. The power curtailment reduces post-fault thermal loading of the critical converter components and even avoids catastrophic failure. Depending on the application and climate conditions, power curtailment after a fault does not necessarily penalize the generated energy. It may be needed just to avoid catastrophic failure during rare moments of peak power generation or processing. Therefore, the zero-redundancy fault tolerance approach suits the best for numerous emerging applications where the cost of implementation is essential while the performance of the post-fault operation is allowed to deteriorate reasonably.

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[PAPER-II] **A. Bakeer**, A. Chub, and D. Vinnikov, "Study of MOSFET Post-Fault Operation in Fault-Tolerant DC-DC Converters," in proc. IEEE 7th International Energy Conference (ENERGYCON), 2022, pp. 1–5, doi: 10.1109/ENERGYCON53164.2022.9830216.

Study of MOSFET Post-Fault Operation in Fault-Tolerant DC-DC Converters

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***Abstract*—This paper investigates the performance of faulty discrete metal-oxide-semiconductor field-effect transistors (MOSFETs) in fault-tolerant high step-up dc-dc converters. This study targets low-power applications where both silicon (Si) and silicon carbide (SiC) technologies could be used at the low- and high-voltage sides, respectively. First, random samples of defective MOSFETs (i.e. for both technologies) were collected from testing real prototypes in the field. The statistics show that Si MOSFETs have 100% short-circuit fault (SCF) as the failure mode, while SiC MOSFETs have 82% SCF probability and 18% open-circuit fault probability. The ohmic resistance of a shorted MOSFET is measured using the impedance analyzer of Keysight E4990A to characterize the behavior of the switches after a fault. Various combinations of short-circuited MOSFETs with different drain-source resistances were used in a real prototype, and the efficiency of the converter was evaluated in each case. The results prove the feasibility of using the short-circuited faulty MOSFET as a conduction path to overcome a SCF.**

***Index Terms*—Fault-tolerant (FT) converters, Discrete power device, MOSFET, Device characterization, Reliability, Physics of failure (PoF).**

I. Introduction

The fault-tolerant (FT) feature becomes essential in power electronic converters with the high penetration of renewable energy sources. In this way, the reliability of power electronic systems can be increased. Fault-tolerant systems can avoid power interruption for critical applications such as data centers and distribution systems (e.g., a smart transformer) [1]. This could be achieved by different approaches such as the overdesign of component, adding redundancy at the component or converter level, or using the topology-morphing control (TMC) with zero redundancy [2]. Additionally, system failures can start with faults of an individual component and lead to total system failure. The literature show that power semiconductor devices are considered the most vulnerable components in power converters, whereas the resistors and inductors have the lowest failure probability [3].

In general, there are two types of failures in power semiconductors: catastrophic failures with constant failure rates and wear-out failures with variable failure rates throughout the lifetime of a component [4]. The former is a random failure rate during the useful lifetime, which can lead to an open-circuit fault (OCF) or short-circuit fault(SCF) in semiconductors. Although the wear-out failure causes a drift in the semiconductor parameters, dc-dc converters do not suffer from this type of failure, as most wear-out damage is caused by thermal cycling that typically appears at the line frequency

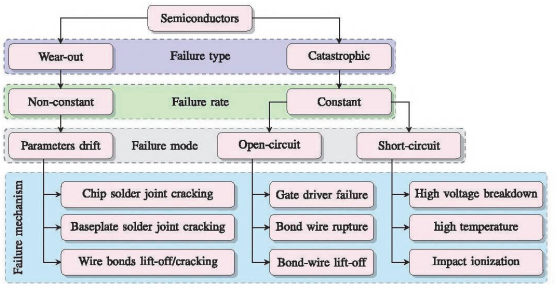

Fig. 1: Failure modes and mechanism of power devices [6]–[9].

in AC systems [5]. The wear-out and catastrophic failures have different failure mechanisms, as depicted in Fig. 1.

Regardless of the failure mechanism leading to catastrophic failure, the fault mode in the power semiconductors is considered to be either OCF or SCF [10]. It is worth mentioning that discrete Si MOSFETs were reported to fail to SCF in 100% cases for all typical failure mechanisms. However, their post-fault resistance values are not consistent and can vary, resulting from ohmic losses influencing temperature in the conducting material and possibly material conversion in the conduction channel [10]. An open-circuit switch can no longer be used in the circuit and is naturally isolated. On the other hand, a switch that fails due to a SCF cannot be controlled by turning the gate on/off, and it can be used in the circuit as a current conducting path after the fault. The ideal short-circuited switch is the one featuring a low ohmic resistance in the range below of its normal $R_{ds,on}$ or even less, so that its losses at the nominal current after a fault do not exceed those in the normal operation [11]. In the case of a non-ideal SCF of the switch, the resistance after the fault exceeds $R_{ds,on}$, which could result in considerable power losses dissipated in the switch, which could eventually lead to an OCF.

One of the promising FT dc-dc converters that has the ability to regulate the input voltage in a wide range is the series resonant isolated buck-boost converter (SRC). It features soft-switching both in the low- and high-voltage bridges and buck/boost functionality at a fixed-switching frequency [12]-[13], which can simplify the magnetic design. In case of the SCF, the FT SRC employs the faulty switch as a current conducting path to reconfigure the faulty inverter bridge from full-bridge to half-bridge SRC, and additional bypass

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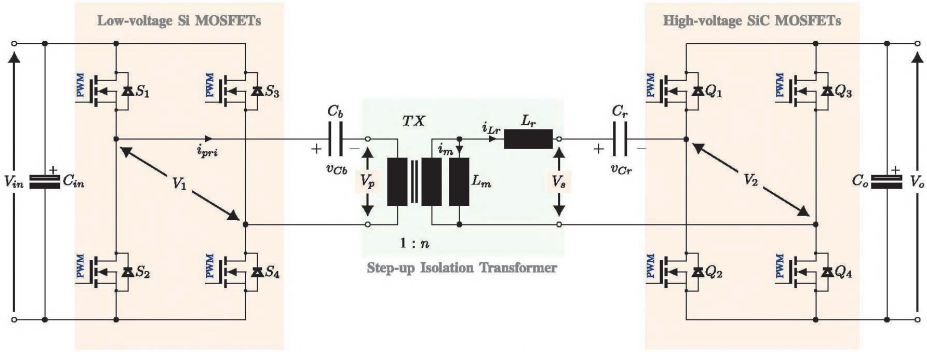

Fig. 2: A bidirectional zero redundancy FT dc-dc converter based on the SRC topology.

switches to reconfigure the healthy bridge [14]. In [15], a new FT SRC implementation using zero redundant components is introduced. Both these FT approaches employ a faulty switch as a current conducting path after the fault occurrence, but only the second approach takes the full advantage of this opportunity to avoid additional redundant components. However, performance of the faulty switches, and resulting converter efficiency, needs to be investigated.

This paper aims to investigate the distribution of the fault types in MOSFETs in the zero redundancy FT SRC. To this end, several defective MOSFETs are eventually soldered into real prototypes. These switches are then classified by fault type to obtain a distribution of fault types for that MOSFET technology. Next, the zero-redundancy FT-SRC performance is experimentally measured on several MOSFETs with different resistances to show the effect on the converter performance after a fault.

The remaining part of the paper starts with Section II describing the case study system used to collect the defective MOSFET samples analyzed in the current study. After that, the fault statistics and experimental results are presented and discussed in Section III. Finally, the conclusions of the paper are drawn in Section IV.

II. Methodology

Figure 2 shows a case study bidirectional FT SRC topology that was implemented in the laboratory and used for experimental tests. Its parameters are listed in Table I.

A batch of faulty devices was accumulated during testing different high step-up dc-dc converters, all of which used 100±5 kHz as the switching frequency and the same power devices at the low- and high-voltage side: surface mounted 100 V/3.5 mΩ Si MOSFET in PG-TDSON-8 case (also known as Power56), and 900 V/280 mΩ SiC MOSFET in TO-247 case. The main parameters of the MOSFETs are summarized in Table II. Control loop instability, mistakes in firmware during initial testing, overheating in critical operating points, load disconnection, not sufficiently tuned protection could be named among typical reasons of converter failures

TABLE I: Parameters of the prototype

Parameter	Symbol	Value
Blocking capacitance	C_b	100 μF
Transformer turns ratio	n	6
Magnetizing inductance	L_m	1 mH
Resonant inductance	L_r	98.5 μH
Resonant capacitance	C_r	27 nF
Resonant frequency	F_r	97.5 kHz
Switching frequency	F_{sw}	95 kHz
Output voltage	V_o	350 V

TABLE II: Parameters of the low- and high-voltage MOSFETs

Parameter	BSC035N10NS5	C3M0280090D
Technology	Si	SiC
Rated voltage [V]	100	900
$R_{ds,on}$	3.5 mΩ	280 mΩ
Rated current [A]	50	22
Gate-source voltage [V]	-5/15	-5/18

during the testing of the pre-industrial prototypes. Since the faulty MOSFETs were collected over a longer period of time, different tests, and different prototypes, it was assumed that the failure mechanism of a defective MOSFET is random.

One phenomenon that has been observed is that surface-mounted Si devices keep mechanical integrity after a fault. Contrary to that, SiC devices working at the high-voltage side could explode, destroying the case integrity and evaporating the semiconductor crystal inside, as demonstrated in Fig. 3. An explosion of a SiC devices results in OCF in all observed cases. On the other hand, the SiC MOSFETs keep mechanical integrity without any visible damage to the case when the SCF occurs.

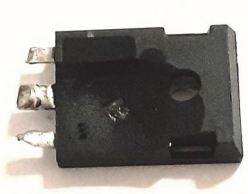

Fig. 3: Example of case damage to a SiC MOSFET featuring OCF.

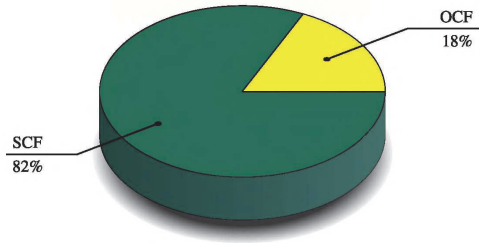

Fig. 4: Distribution of the fault type in high-voltage SiC MOSFETs.

III. Results and Discussion

First, the drain-source and gate-source low-resistance connections were identified in all faulty MOSFETs using a multimeter Fluke 179 to determine the failure modes of the faulty MOSFET. The total number of low-voltage Si MOSFETs is 32 switches, where SCF stands for 100% of the dataset. The main reason could be the high current stress typical for the low-voltage side of high step-up dc-dc converters. On the other hand, the distribution of OCF and SCF of the high voltage SiC MOSFET is shown in Fig. 4. It is clear that is the dominant failure mode of high-voltage SiC MOSFETs in the given type of dc-dc converters. The resulting statistical analysis of the data set is consistent with the statistical results collected for the series resonant converters in industrial applications in [1]. It is worth mentioning that the initial batch of faulty Si 100 V MOSFETs also contained a significant number of switches (roughly forty) featuring the short-circuited gate and source leads. They were excluded from this study due to issues with auxiliary supply protection in the prototype. In reality, the gate driver of the MOSFET should be protected against the short-circuit and avoid auxiliary power supply interruptions. Nevertheless, all those switches had shorted the drain-source.

It is important to analyze the impedance behavior of a short-circuited MOSFET when it is considered as a post-fault current conduction path. Several short-circuited faulty MOSFETs were placed in the prototype instead of healthy ones and loaded for 40 hours. Their resistance remained unchanged, even though they were loaded with maximum current stress at the switching frequency. Keysight E4990A impedance analyzer was used to measure the resistance for both Si and SiC MOSFETs. In all measurements, the post-SCF was virtually independent of the measurement frequency.

Measurement results show that for both semiconductor technologies, SCF switches could be broken down into two groups: those with nearly ideal post-SCF resistance that is close to the normal $R_{ds,on}$, while the majority of the SCF switches feature post-SCF resistance that is one order of magnitude higher than the normal $R_{ds,on}$. This observation is different from that in [11].

Fig. 5 present four examples that demonstrate this observation. For Si MOSFETs, post-SCF resistance is rarely below 10 mΩ (see example in Fig. 5a), while most of the cases fall randomly between 30 mΩ and 90 mΩ (see example in Fig. 5b). A somewhat different situation was observed for SiC MOSFETs featuring SCF. The majority of cases demonstrated nearly ideal short-circuit when the post-SCF resistance is much below the normal $R_{ds,on}$, as shown in Fig. 5c. However, several cases show post-SCF resistances that are one order of magnitude higher than the normal $R_{ds,on}$, as exemplified in Fig. 5d.

When measuring the post-SCF resistance of one SiC MOSFET, an unusual impedance value of 36.8 Ω was observed. To better understand the nature of this SCF, it was tested under a load condition of 2 A for thirty hours to verify the stability of its high impedance. This ample was suffering from very high ohmic losses, resulting in the resistance increase to 41.20 Ω. This behavior is in line with the prediction given in [11], where the authors assume that excessive losses cause further conversion of conducting material to high-impedance state. This means that the switch failure status can change from an SCF to OCF over time. On the other hand, such excessive power dissipation is likely to destroy PCB before OCF can be achieved.

It is important to emphasize, that in the case of post-SCF resistance 10-30 times higher (according to our measurements) than the normal $R_{ds,on}$, power losses in such a MOSFET could be comparable to its maximum power losses in the normal operation conditions, or even exceed them. There are two possible solutions to this issue:

- predict and consider possible excessive power losses during the converter thermal design;
- curtail power if internal thermal sensor of the converter shows excessive heating inside a potted enclosure.

The second approach provides a lower converter cost while improving the reliability of the remaining healthy components by avoiding operation at peak powers.

The efficiency of the FT SRC prototype was measured in both health and faulty status at different power levels in an open-loop operation are given in Fig. 6. The light-load efficiency is relatively low in the normal mode, as the full-bridge design is more optimized for full-power operation. The converter achieves a peak efficiency of 97.60% in the normal operation at higher power, where the converter component is overloaded in the post-fault operation. On the other hand, after a reconfiguration much fewer components are processing the converter power, which results in increased light-load efficiency (below 150 W), but decreased full-power efficiency [15]. Several combinations of post-fault scenarios were considering using the switches measured in Fig. 5. It is clear

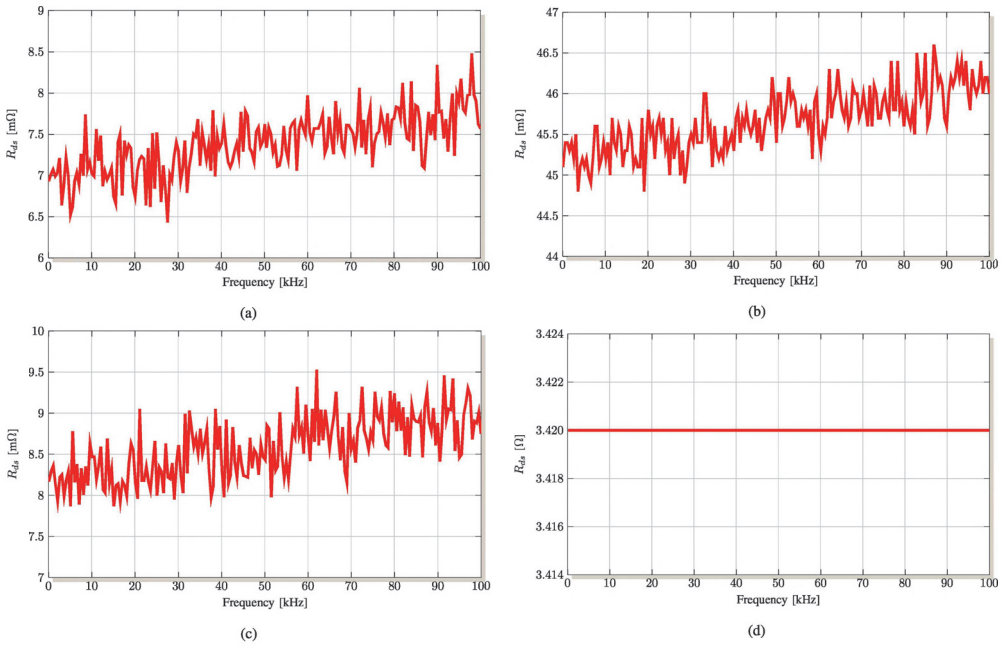

Fig. 5: Post-SCF drain-source resistance measurement results of four failed MOSFETs: a) low-resistance Si, b) high-resistance Si, c) low-resistance SiC, and d) high-resistance SiC.

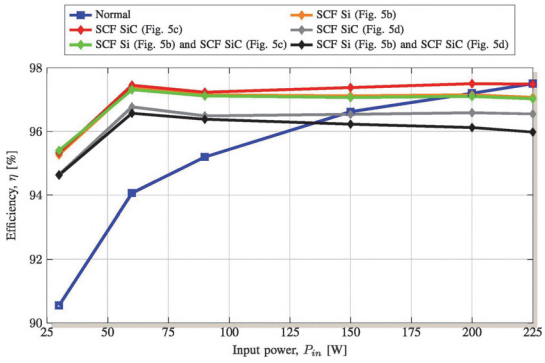

Fig. 6: Experimental efficiency of the FT SRC in the normal and post-fault operation mode with different combinations of faulty MOSFETs at the input and output sides.

that MOSFETs with non-ideal post-SCF resistance degrade the efficiency of the converter much more than those with nearly ideal shorting. Scenarios considering the SiC MOSFET with high post-SCF resistance show the lowest efficiency dues to high conduction losses in that switch.

IV. Conclusion

This paper investigates the characteristics of MOSFETs after failure and their influence on performance of fault-tolerant dc-dc converters. Two types of MOSFETs Si and SiC are tested as they correspond the best to designs of high step-up galvanically isolated dc-dc converters. The SCFs are the dominant in SiC MOSFETs, while Si devices feature only SCF due to high current stress at the low-voltage side.This study shows that only a small fraction of Si MOSFETs show post-SCF resistance comparable to the normal $R_{ds,on}$. SiC MOSFETs show low post-SCF much more often, but some of them also show very high resistance after a fault.

Therefore, the zero-redundancy fault tolerance concept can be considered feasible as the faulty switch can be used as a current conducting path in a reconfigurable fault-tolerant dc-dc converter. However, such a converter should be thermally designed to withstand high ohmic losses in shorted MOSFETs. Alternatively, its control system should implement a power curtailment algorithm limiting stresses of remaining healthy components after a fault as well as overheating of a SCF switch used as a current conduction path in a reconfigured dc-dc converter.

The future research will focus on experimental implementation of zero redundancy fault tolerant dc-dc converter with closed-loop control systems including fault detection and remedy.

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[PAPER-III] **A. Bakeer**, A. Chub, and D. Vinnikov, "Short-Circuit Fault Detection and Remedial in Full-Bridge Rectifier of Series Resonant DC-DC Converter Based on Inductor Voltage Signature," *in proc. IEEE 61st International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2020, pp. 1–6, doi: 10.1109/RTUCON51174.2020.9316482.

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Short-Circuit Fault Detection and Remedial in Full-Bridge Rectifier of Series Resonant DC-DC Converter Based on Inductor Voltage Signature

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***Abstract*— This paper proposes a method to detect the short-circuit fault (SCF) in the full-bridge diode rectifier at the output side of the series resonant dc-dc converter (SRC). The full-bridge inverter is employed at the input side. The utilized diagnostic/signature signal to detect the SCF is the voltage of the resonant inductor, which increases after fault occurrence. Also, sensing the inductor voltage is an easy way through inserting a few turns into the core of the resonant inductor without affecting its operation. The sensed inductor voltage is compared with a threshold voltage, which is calculated based on the converter parameters. After the identification of the SCF fault, the input-side bridge is reconfigured into a half-bridge structure to recover the normal operation of the converter because the output side is operating as a voltage doubler in this case. Since in the proposed method, localization of the exact faulty diode is not considered important in the further operation, fast recovery of the fault condition can be achieved. The simulation results provided show the feasibility of the detection algorithm and the remedial action at different operating conditions.**

***Keywords*— Series resonant converter; fault tolerance; fault detection; full-bridge rectifier; reliability.**

I. Introduction

Power converters have spread into many applications in our life, and their reliability has received close attention to minimize the fault effect as much as possible. Reliability is considered an important factor, especially for critical applications, such as aircrafts, data centers, and medical devices [1]. According to the industrial statistics on the probability of fault occurrence in the components of power converters, power semiconductors are considered the most vulnerable components that contribute approximately 40% of all fault cases [2]. Power switches are a major source of the semiconductor faults since their electrical and thermal stresses are usually highest [3]. However, faults of the diodes could destroy the converter after a certain time from the fault occurrence as they can result in consequent faults of the power switches.

Technically, fault types in the semiconductors of the power converter could be generally classified into two types: open-circuit fault (OCF) or short-circuit fault (SCF) [4]. OCFs could result from drive failure, solder fatigue, or bond wire lift-off [5]. OCF can take a long time without detection and remedial, and the converter does not face a serious problem. On the other hand, if the SCF is not detected and isolated fast enough, the converter could be destroyed within a short time. SCFs often result from improper gate-driver or intrinsic failure due to the overvoltage stress or temperature stress [1].

In the detection of the fault (OCF or SCF), the diagnostic signal (i.e., signature signal) should be well selected to ensure provision of adequate information about the operation of the converter. The diagnosis methods of fault detection vary in such aspects as detection speed, number of sensing signals, computational effort, comprehensive fault detection, and cost of implementation. Also, these methods could be classified into model-based and signal-based. For the former model-based method, estimation techniques were used to find the normal trajectory of the diagnostic signal and compare it with the measured one from the converter. The deviation between the estimated and the measured values compared to a threshold value with additional tolerance refers to a faulty case. The most common estimators are based on Kalman filter [6], sliding mode observer [7], or adaptive observer [8].

On the other hand, a fault could be identified based on signal-based methods to extract the features that show the faulty case from the measured signals [9]. The diode voltage has been used as a signature signal in the isolated converters beside the gating signal of the main switch [4]. In the phase-shifted full-bridge (PSFB) converter, the transformer voltage and the dc input current are chosen as the signature signals to detect and locate the SCF in [3]. In [10], the magnetic field of the diagnostic signal is analyzed using the Fast Fourier Transform (FFT); however, this approach has the drawback of high computational burden. In the current studies, fault detection and remedial with the modular multilevel are frequently addressed, and the capacitor voltage of each submodule cell in the arms is utilized as the diagnostic signal, which needs many sensors with an increasing number of levels [11].

One of the promising power converters for the wide-range voltage regulation is the series resonant dc-dc converter (SRC). This topology features soft-switching and high efficiency. The output-side rectifier of the SRC could be implemented with different rectifier cells [12]-[17]. To improve the efficiency of the converter, the resonant

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inductance can be optimized. Usually, an external inductor is used to compensate for the low leakage inductance of the isolation transformer. This study addresses the SRC implementation with a resonant tank featuring quality factors much less than one to reduce the size of the inductive components. Therefore, the switching frequency should be selected close to at least 5% from the resonant frequency to ensure full zero voltage switching (ZVS) for the primary semiconductors at the nominal input voltage. Proper dimensioning of the magnetizing inductance enables ZVS regardless of the value of the load power as the magnetizing current is independent of the operating power.

This paper aims to improve the reliability of the dc-dc converter based on the SRC against the SCF in the output-side rectifier. The considered topology utilizes the full-bridge diode-based rectifier. Also, the converter is operating as a dc transformer at the nominal input voltage and generates the output voltage of 350 V, which is suitable for dc microgrid applications. The inductor voltage, which begins to increase after the fault occurs, is selected as the diagnostic signal because sensing the inductor voltage is considered an easy way through inserting a few turns into the resonant inductor core with a negligible side effect on the resonant tank operation. A simple analog circuit has been designed to compare the inductor voltage with the threshold value. After the fault detection is triggered, removal of the fault is obtained by reconfiguring the converter without the need to exactly find the location of the faulty diode. By using the proposed fault tolerance strategy based on reconfiguring the input-side bridge into a half-bridge, the converter operation can be continued after the SCF occurs in the output-side diodes. Section II describes the proposed methodology; the simulation results are discussed in Section III, and the conclusions are drawn in Section IV.

II. Proposed Fault Detection And Fault Tolerance Methodology

A. Description of the Topology

The studied converter based on the SRC topology is presented in Fig. 1. The input-side bridge consists of four MOSFETs S_1-S_4 operating complementary with a phase shift of 180 degrees, which could reduce the circulating current in the circuit [18]. A short dead-time is inserted between the gating signals of the two MOSFETs in each leg to avoid the short-circuit across the input supply.

The input-bridge provides a static conversion gain close to one. The isolation transformer serves to boost the input voltage by the factor of the turns ratio n and provides galvanic isolation. The resonant tank parameters of L_r and C_r feature sinusoidal current along the switching period as long as the converter does not enter into the free-wheeling state.

The average voltage of the resonant capacitor equals zero, and the peak voltage of C_r depends on the converter power P_{OUT} and the input voltage V_{IN} as

$$\Delta V_{Cr} = \frac{P_{OUT} T_{SW}}{4 n V_{IN} C_r} \quad , \tag{1}$$

where T_{SW} is the switching period.

The following assumptions were set to simplify the analysis of the proposed fault detection algorithm:

1. The output voltage V_{OUT} is constant and almost ripple-free as the capacitance of the decoupling capacitor C_O is high.
2. The leakage inductance of the transformer is small compared to the external resonant inductance.
3. The dead-time in the PWM scheme of the primary side switches is small and could be ignored.

B. Selection of the Diagnostic Signal

It is essential to select a diagnostic signal that has much information related to the converter status and easy to implement. Using the inductor voltage as the diagnostic signal is beneficial; this solution is of lower cost for it requires only adding a small winding of a few turns into the resonant inductor core. Besides, these inserted turns do not affect the operation of the inductor as they are loaded with a sensing circuit drawing very low power. Also, the voltage of the inductor responses to the diode SCF in the corresponding half-cycle when the current increases due to the SCF occurrence. The study in [19] proposed a methodology to use the inductor voltage to detect the fault, but it requires the gating signal of the switching pattern in the case of the forward converter. Unlike this algorithm, here we use only the inductor voltage without the need for additional signals. Neither is there any need to localize the faulty diode in the output-side rectifier for the proposed method as the same remedy action will be applied.

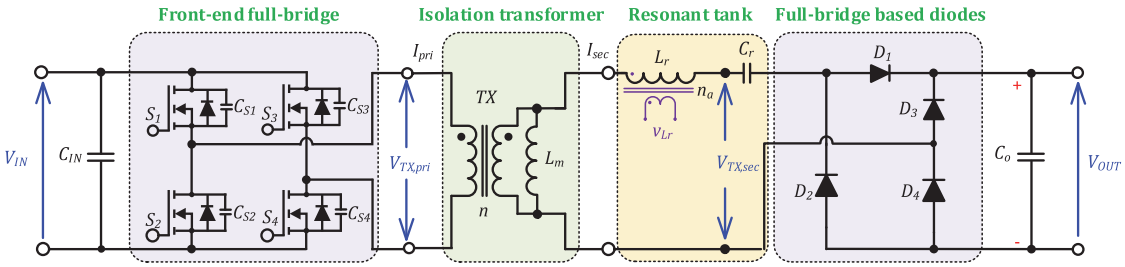

Fig. 1. The studied topology of the SRC with the full-bridge rectifier based on diodes in the output side.

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The equivalent circuit of the converter during normal operation is given in Fig. 2(a) for the positive half-cycle. The peak value of the voltage across L_r equals ΔV_{Cr} in the healthy condition. If the SCF occurs in D_1 or D_4 during the positive half-cycle, or in D_2 or D_3 during the negative half-cycle, the converter is still running in the normal operation till the next half-cycle (negative/positive) where the effect of the SCF will be evident. Further description of the proposed fault detection algorithm considers the case study when an SCF occurs in D_2 during the positive half-cycle. With the SCF in D_2, the inductor voltage v_{Lr} features a high value provided by the equivalent voltage of the transformer secondary winding and the capacitor voltage, as shown in Fig. 2(b). The response of the inductor voltage before and after the SCF occurrence is shown in Fig. 3, where S_1 is the gating signal of the MOSFET S_1. After the SCF occurrence, the output-side rectifier is operating similar to the well-known Greinaher voltage doubler rectifier.

C. Detection Algorithm of the Short-Circuit Fault

The threshold value of the inductor voltage should be defined with some tolerance, as this value will be constant for the whole range of operating conditions. Ideally, the peak of the resonant inductor voltage equals the peak value of the resonance capacitor voltage ΔV_{Cr}, and the value of ΔV_{Cr} has the maximum value at the rated power and minimum input voltage (1). At this condition, ΔV_{Cr} has the maximum possible value within the whole converter range of operation. The flowchart of the proposed detection algorithm is shown in Fig. 4.

A simple low-cost analog circuit to implement the proposed SCF detection is given in Fig. 5. The sensed inductor voltage is a bipolar signal, so it is better to rectify it using the low-power full-bridge rectifier. Then, the rectified signal is filtered using the low pass filter, which is used to remove the spike in the inductor voltage at reversing the direction of the resonant current. It is comprised of R_1 and C_1, and the filtered signal is v_{Lrf}. The threshold voltage can be adjusted using the potentiometer R_3. The output of the comparator circuit is a digital signal that feeds the controller. Table I summarizes the comparator output as a function of the filtered signal v_{Lrf} and V_{th}.

TABLE I: OUTPUT OF THE ANALOG CIRCUIT

Condition	*S*	Converter Status
$v_{Lrf} \leq V_{th}$	Low	Healthy state
$v_{Lrf} > V_{th}$	High	Faulty state

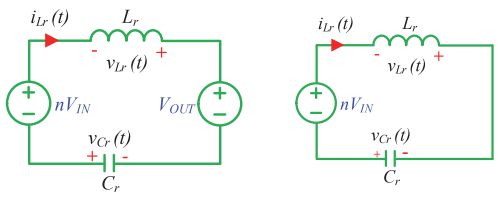

Fig. 2. Equivalent circuits of the converter in the positive half-cycle at (a) healthy condition and (b) SCF of the diode D_2.

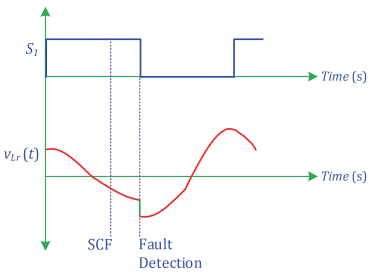

Fig. 3. Sketch of the diagnostic signal (i.e., inductor voltage) before and after the SCF occurrence.

D. Fault-Tolerance of the Converter

This stage aims to continue the operation of the converter after the fault occurrence through rearranging the converter structure. If the SCF does not remedy, the output voltage of the converter becomes double because the converter is operating as a voltage doubler in the output side. Also, the average voltage of the resonance capacitor equals half of the output voltage. To keep the same gain of the converter, the primary voltage of the transformer should be reduced by half after the fault detection. Therefore, the transistor S_3 is turned off, while the switch S_4 is always turned on. Also, the primary MOSFETs S_1 and S_2 are driving with the same methodology in the healthy state. Accordingly, the schematic of the input-side is a half-bridge after the reconfiguration, as shown in Fig. 6. With the proposed reconfiguration, the total gain of the converter before and after the fault occurrence is the same. Furthermore, there is no further need of the proposed detection method for the fault localization as the same action of the topology reconfiguration is applied whatever location of the faulty diode in the output-side rectifier.

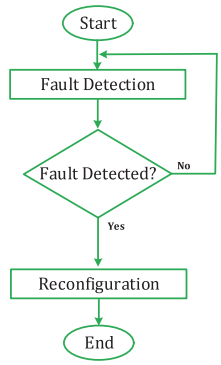

Fig. 4. Flowchart of the detection algorithm.

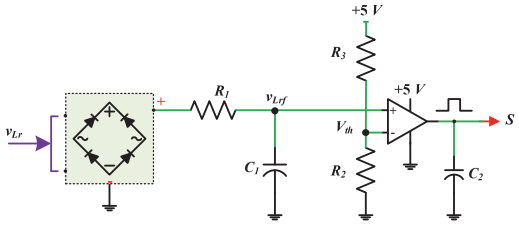

Fig. 5. Hardware implementation of the proposed fault detection method.

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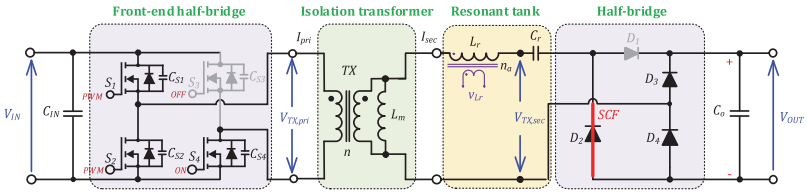

Fig. 6. Reconfiguration of the converter after the SCF detection at D_2.

III. Simulation Results And Discussion

The converter with the proposed fault detection and tolerance strategies was simulated using the PSIM software; the parameters of the converter are listed in Table II. Commonly, the output voltage of the SRC is changed when the quality factor changes, i.e., the load changes, so the input voltage is adjusted to maintain the output voltage of the converter fixed at 350 V. The parasitic effects are included in the model to make sure the proposed method will function in the real converter.

Table II. Simulation Parameters

Parameter	Symbol	Value
Input voltage range	V_{IN}	45:60 V
Input side capacitor	C_{IN}	150 µF
Transformer turns ratio	n	6
Magnetizing inductance	L_m	1 mH
Resonance inductance	L_r	96.5 µH
Detection turns ratio	n_a	30:1
Resonance capacitor	C_r	30 nF
Output side capacitor	C_O	150 µF
Output voltage	V_{OUT}	350 V
Switching frequency	F_{SW}	95 kHz

A. Short-circuit Fault at Light-Load Condition

At a light load, the resonant current as well as the inductor voltage are very low, and the voltage of the capacitor C_r is low according to (1). Therefore, this scenario can test the sensitivity of the proposed algorithm in the worst condition. The simulation results during this condition are shown in Fig. 7. The input voltage is adjusted at 46 V, and the value of the resistive load is 4083.5 Ω, i.e., P_{OUT} = 30 W. The capacitor voltage based on (1) equals approximately 10 V. The inductor current shape is distorted due to the influence of the parasitic capacitances of the diodes and its peak value equals 2 A before the fault occurs at the instant 0.04 s.

After the SCF occurs in the diode D_2 at the instant 0.04 s, the inductor voltage takes less than one switching period to reach the threshold level. The detection algorithm identifies the faulty state within roughly 0.6 µs, and the converter is directly reconfigured by turning on the switch S_4 and turning off the switch S_3. It is clear that the output voltage is constant at 350 V after the converter reconfiguration, and the output side rectifier is operating as the voltage doubler.

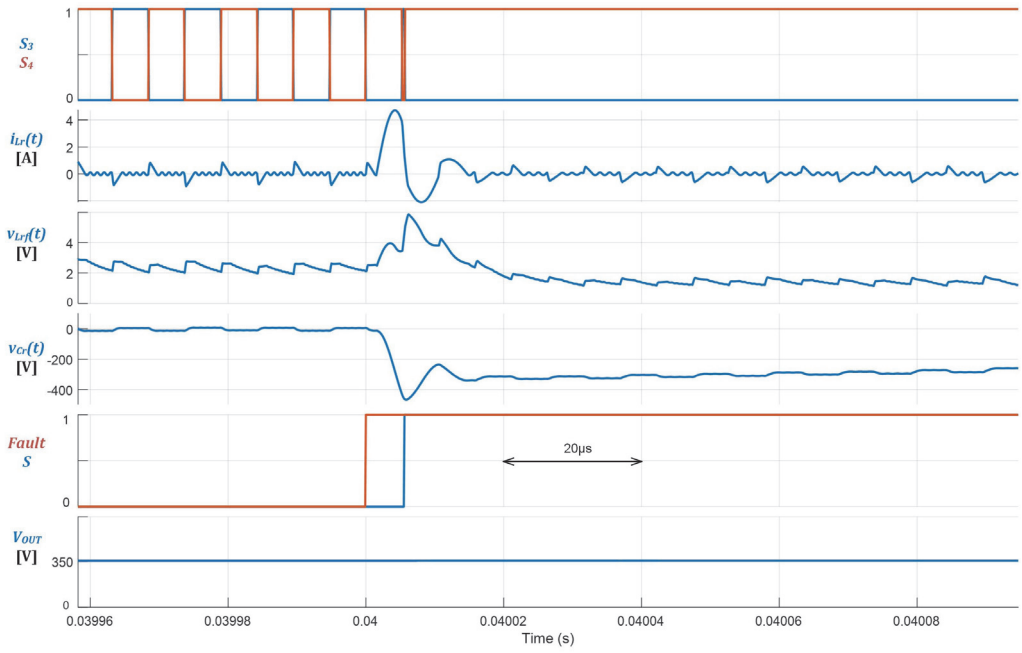

Fig. 7. Simulation results at the light-load condition with SCF in D_2.

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B. *Short-Circuit Fault at Full-Load Condition*

The input voltage equals 57 V, and the converter is loaded with full power at 200 W, i.e., the value of the resistive load equals 612.5 Ω. The simulation results are shown in Fig. 8. The peak of the capacitor voltage is 51.50 V based on (1). The DCM period is smaller than in the previous condition at the light-load, and the output-side diodes are turned off at a zero current switching (ZCS). The diode D_2 is shorted at the instant 0.04 s, and the fault detection circuit identifies the fault within 0.54 µs after the capacitor voltage is reaching the threshold voltage V_{th} within less than one switching period. The voltage is approximately constant after the fault occurs, as shown in Fig. 8. It can be noted that both state-variables of $i_{Lr}(t)$ and $v_{Cr}(t)$ have an approximately sinusoidal profile.

IV. Conclusion

The paper has presented a methodology to detect the short-circuit fault in the output-side rectifier diodes of the SRC. The diagnostic signal is selected based on the resonant inductor voltage that is easy to implement. The proposed detection algorithm can identify the faulty status in less than one switching period. Also, the diagnostic signal can detect the SCF in the rectifier diodes without adding more sensing signals. The simulation results prove the effectiveness of the proposed fault detection methodology at different operating conditions. Future work will consider experimental validation of the proposed methodology in high step-up applications.

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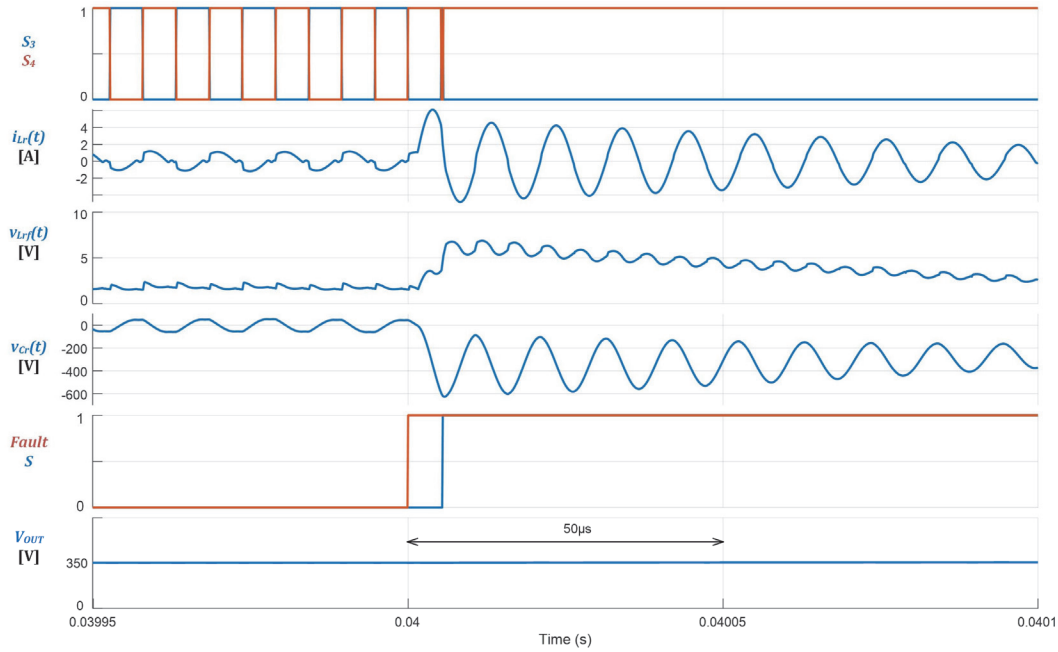

Fig. 8. Simulation results at the full-load condition with SCF in D_2.

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[PAPER-IV] **A. Bakeer**, A. Chub, A. Blinov, and J.-S. Lai, "Wide Range Series Resonant DC-DC Converter with a Reduced Component Count and Capacitor Voltage Stress for Distributed Generation," in Energies, vol. 14, no. 8, MDPI AG, p. 2051, Apr. 07, 2021. doi: 10.3390/en14082051.

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Article

Wide Range Series Resonant DC-DC Converter with a Reduced Component Count and Capacitor Voltage Stress for Distributed Generation

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Abstract: This paper proposes a galvanically isolated dc-dc converter that can regulate the input voltage in a wide range. It is based on the series resonance dc-dc converter (SRC) topology and a novel boost rectifier. The proposed topology has a smaller number of semiconductors than its SRC-based existing topologies employing an ac-switch in the boost rectifier. The proposed dc-dc converter comprises only two diodes and one switch at the output side, while the existing solutions use two switches and two diodes to step up the voltage. The proposed converter boosts the input voltage within a single boosting interval in the positive half-cycle of the switching period. In addition, the resonant current in the negative half-cycle is sinusoidal, which could enhance the converter efficiency. The resonant capacitor voltage is clamped at the level of the output voltage. Therefore, the voltage stress of the capacitor could significantly reduce at various input voltage and power levels. This makes it perfect for distributed generation applications such as photovoltaics with wide variations of input voltage and power. The converter operates at the fixed switching frequency close to the resonance frequency to obtain the maximum efficiency at the nominal input voltage. The zero-voltage switching (ZVS) feature is achieved in the primary semiconductors, while the diodes in the output-side rectifier turn off at nearly zero current switching. The mathematical model and design guidelines of the proposed converter are discussed in the paper. The experimental results confirmed the theoretical analysis based on a 300 W prototype. The maximum efficiency of the converter was 96.8% at the nominal input voltage, and the converter has achieved a wider input voltage regulation range than that with the boosting cell comprising an ac-switch.

Keywords: series resonant converter (SRC); wide range voltage regulation; bidirectional switch; conversion efficiency

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1. Introduction

With the rapid growth in the installation of photovoltaic (PV) modules in residential settings worldwide, the demand for new power converters with high efficiency and low cost is increasing [1]. This trend is expected to be complemented with the wider use of dc microgrids [2]. As a result, dc-dc converters are required to connect PV modules to a dc-bus of a dc-microgrid [3]. These converters have to maintain the following specifications: high power density, high efficiency, regulation of the wide range of variation in the input voltage, and compact size [3].

The converter with a wide input voltage regulation range could be capable of tracking the maximum available power of the PV module in various environmental and shading conditions. One of the promising candidates for this purpose is resonant converters like LLC [4–6] and the series resonant converter (SRC) [7–9], which are used in many

industrial applications. However, LLC employs frequency modulation to regulate the voltage variation, and thus the design of the magnetic component becomes costly and complicated. The SRC has received more attention thanks to its simple design and control. Its implementation allows the resonant current to be discontinuous, i.e., the quality factor of the resonant tank is less than one. This implementation could perform the buck and boost functionality using different pulse width modulation (PWM) schemes with boost rectifier cells. The buck regulation requires the use of a special modulation at the input side, while the boost regulation requires a boosting rectifier cell, regulating the transformer leakage inductance current at the output side [10]. In addition, it can regulate the voltage while operating at a fixed switching frequency by adjusting the duty cycle of the semiconductors. Additionally, the voltage regulation range of the SRC depends on the switching cells utilized in the input and output sides [10–12]. This study is focused on the boost voltage regulation in the SRC using a boosting rectifier cell.

The boosting capabilities of the SRC can be upgraded by developing new boosting cells to be used at the output side. Since the resonant current on the high voltage side is relatively low, integrating the boosting cell on the secondary side of the isolation transformer minimizes losses. There are different investigated cells for the SRC aiming to improve the converter efficiency and the regulation range [13–17]. The bridgeless rectifier cell with two diodes and two metal oxide semiconductor field-effect transistors (MOSFETs) has been used widely in power factor correction applications. It has been used in [13], to step up the input voltage. Recently, it was demonstrated, in [11], that its regulation range is limited due to the possibility of reverse current flows in the same half-cycle due to the parasitic current path caused by the overlapped PWM scheme. The boosting cells in [14,15] have different PWM schemes, where the latter employed synchronous rectification to improve efficiency at the expense of cost and control complexity. In [16], the voltage boosting interval appears only at one half-cycle, and consequently, the resonance current has a sinusoidal waveform in the other half-cycle of the switching period, which avoids one hard turn-on of a transistor in the boosting cell. The configuration of the circuit in [17] employs two switches and two diodes. To implement the ac-switch, the two switches are connected as a back-to-back structure. In addition, two diodes and two capacitors are implemented with the voltage doubler rectifier. Contrary to the other boosting cells, the leakage inductance current rises linearly during the boosting interval like in the conventional boost converter. Although this boosting rectifier cell has a lower voltage stress on the MOSFETs and could reduce the switching losses, the voltage regulation range is substantially limited, especially at higher resonance inductance [12].

This paper modifies the boosting rectifier cells from [17], by removing one switch and rearranging the other switch and two diodes. Consequently, the proposed cell comprises only one MOSFET and two diodes in the configuration of the rectifier cell. The voltage stress on the resonance capacitor is clamped at the output voltage level, whatever the input voltage and power level. This resolves the main issue of the counterpart cells that could suffer from excessive stress on the resonant capacitor in case of overloads and regulation transients. In low-power conditions and lower dc voltage gains, the derived SRC employs only one diode, where the other diode is in the idle state. The modulation scheme applied to the proposed topology employs the forced half-resonance to enhance converter efficiency as the current has a half-wave sine waveform in one half-cycle of the switching period. The proposed circuit has various modes of operation that enable the converter to cope with the wide range of input voltages and power variations that are common for distributed generation applications. This paper will only handle regulating the low-input voltage, i.e., boosting condition.

The remaining content of the paper starts with Section 2 that comprehensively describes and analyzes the operation of the proposed topology in the boost mode, where the proposed boosting cell is used at the output side. Section 3 introduces the design guidelines and experimental results of the converter. Finally, Section 4 concludes the paper.

2. The Proposed Converter

2.1. Description of the Topology

The proposed topology is shown in Figure 1. The input capacitor, C_{IN}, filters out the converter input current ripple and decouples the input voltage source, V_{IN}. The front-end full-bridge comprises the semiconductors S_1–S_4 operating as a high-frequency inverter. The isolation transformer, TX, is employed to step up the input voltage by the factor of the turns ratio, n. It also provides galvanic isolation between the input and output sides to increase the safety level. The magnetizing current of the transformer, I_m, which corresponds to the magnetizing inductance, L_m, helps achieve the soft-switching of the input-bridge semiconductors, as will be discussed later. The sum of the leakage inductance of the transformer, L_{lk}, and the external resonant inductance, L_{ext}, represents the resonance tank inductance, $L_r = L_{lk} + L_{ext}$. As a result of the magnetic integration of the isolation transformer and the resonant inductance, the size and cost of the converter will be decreased.

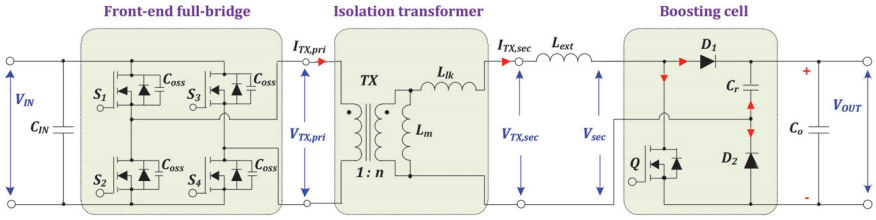


Figure 1. Configuration of the proposed topology of series resonance dc-dc converter (SRC) with a single-switch boosting rectifier cell.

The resonance frequency of the converter, F_r, is defined in (1), where C_r refers to the resonant capacitance of the resonant tank. The boosting cell of the converter includes one MOSFET Q and two diodes (D_1 and D_2). The gating signal for Q must be adjusted regarding the biased state of the top diode D_1. Next, the rectified voltage from the boosting cell is smoothed by the decoupling output capacitor, C_O. The converter operates at a fixed switching frequency, F_{SW}, which has to be selected at 5–10% lower than the resonance frequency to obtain the possible high conversion efficiency under the nominal input voltage [13].

$$F_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

The peak-to-peak voltage ripple value of the resonant capacitor, ΔV_{Cr}, can be defined as in (2). Although ΔV_{Cr} is mainly affected by the power level and input voltage of the converter, the maximum voltage across C_r does not exceed the value of the output voltage, V_{OUT}, because the capacitor voltage will be clamped by the conducting bottom diode D_2. In addition, the relation in (2) will not be valid in these conditions, and thus the maximum ripple this value cannot exceed $\Delta V_{Cr(max)} = 2nV_{IN}$. Therefore, the voltage stress of C_r is reduced at high power compared to the existing boosting rectifier cells. It is worth mentioning that D_2 does not conduct as long as the capacitor voltage is less than the output voltage at any given time. The subsequent analysis of the proposed topology will be set according to these observations. The converter operation conditions depend on the operating point of the output power and the input voltage, as will be discussed later.

The following considerations are made to make the analysis simpler:

1. Each primary side semiconductor has a parasitic output capacitance of C_{oss}, while the other converter components are ideal;
2. Negligible output voltage ripple;
3. The output capacitance C_O is much larger than C_r;
4. The converter is lossless;

5. The state variables of the converter are the resonance inductor current, $i_{Lr}(t)$, and the resonance capacitor voltage, $v_{Cr}(t)$.

$$\Delta V_{Cr} = \frac{P_{OUT} T_{SW}}{2nV_{IN} C_r}, \tag{2}$$

where P_{OUT} is the load power, and T_{SW} is the switching period of the converter.

2.2. Modes of Operation

The operation and design of the proposed converter are based on the discontinuous resonant current conditions in the case when the quality factor of the resonant tank is less than one under any load [10].

2.2.1. Operation at the Nominal Input Voltage (*Pure-SRC*)

As was mentioned in the Introduction, the SRC can operate both in the buck and boost modes. The operating point between them corresponds to the nominal input voltage when the given converter operates as a conventional non-controlled fixed-gain SRC with a purely sinusoidal current of the resonant tank. This is the normal state of the converter operation at which the output voltage is generated only by the boosting action from the isolation transformer. It will be referred to as *pure-SRC* in the remaining part of the paper. The equivalent circuit corresponds to a voltage doubler in the output-side cell with a single resonant capacitor.

The steady-state waveforms of the proposed converter are given in Figure 2. The diode D_2 remains reverse biased during this condition where $v_{Cr}(t) < V_{OUT}$ at all the levels of the converter power. Thus, the current of the bottom diode equals zero, as shown in Figure 2. The switch Q duty cycle equals 0.5, excluding the short dead time. The value of ΔV_{Cr} can be accurately defined by Equation (2). The trajectory curve is close to a circular shape due to the sinusoidal contour of the resonance current and the capacitor voltage, as shown in Figure 3. The vertical axis corresponds to the resonant current multiplied by the characteristic impedance of the resonant tank, Z_r. The resonant current reaches its maximum value when the resonant capacitor voltage equals zero and vice versa.

The transistor Q gate signal follows that of the switches S_2 and S_3 to ensure that the top diode D_1 is conducting during the positive half-cycle. When a positive voltage is applied to the transformer primary windings, the magnetizing current of the transformer, I_m, has a positive slope and vice versa. The peak value of $I_{m(max)}$ depends on the input voltage and switching period as in (3). During the dead time between the switches in the same leg, the magnetizing inductance acts as a current source reflected onto the primary side to charge/discharge the parasitic output capacitance of the semiconductors, C_{oss}. If the dead time is long enough, the primary switches are turned on at zero voltage switching in the next switching half-cycle. The diode D_1 is turned off at nearly zero current switching at the end of the positive half-cycle as the resonance current drops down to zero and the converter enters the freewheeling state. The duration of the resonant current pulse feeding the load during the positive half-cycle depends on the operating power of the converter. At the same time, it occupies all the negative half-cycle due to the switch Q being turned on during this half-cycle.

$$I_{m(max)} = \frac{T_{SW}}{4nV_{IN} L_m} \tag{3}$$

2.2.2. Operation at the Input Voltages below the Nominal (*Boost-SRC*)

If the input source of the converter is a photovoltaic (PV) module, as an example, the terminal voltage is decreased under partial or opaque shading conditions. The reduced input voltage must be stepped up to the target dc-bus voltage by the converter. Therefore, the transistor Q is controlled with a duty cycle larger than 0.5 and uses the resonance inductor to boost the secondary winding voltage. During the conduction time part exceeding half of the switching period, the leakage inductance current is increasing, storing

energy supplied from the input source. These operation conditions will be referred to as *boost-SRC* in the text below. There are three possible scenarios of the converter operation in the *boost-SRC* conditions: A, B, and C, depending on the critical time, t_{cri}, at which the instantaneous value of the capacitor voltage reaches the output voltage starting from the beginning of the positive half-cycle. The steady-state waveforms and the trajectory curves of the state variables of the converter are given in Figures 4 and 5, respectively, for three operation scenarios. During the *boost-SRC* condition, the converter will operate in the following modes:

Mode I [$t_0 < t \leq t_1$] (first part of the boosting interval): This represents the starting of the positive half-cycle as the transformer's primary winding has a positive voltage by turning on the switches S_1 and S_4 at the instant $t_0 = 0$. This instant will be used as a reference in all three operation scenarios for the *boost-SRC* conditions. The initial value of the resonance current is zero from the end of the previous half-cycle. Meanwhile, the capacitor voltage has an initial value of $v_{Cr}(t_0)$. The MOSFET Q continues conducting from the previous (negative) half-cycle. The top diode D_1 is reverse biased when the switch Q is conducting, while the anode–cathode voltage across the bottom diode D_2 is negative as $v_{Cr}(t)$ is lower than V_{OUT}. Therefore, D_2 is reverse biased from the instant t_0 as well. The equivalent circuit of the converter in this mode is depicted in Figure 6a for clarity. L_r and C_r are always resonating during this mode and start charging in a positive direction. The current charging profile of L_r follows the sinusoidal waveform. The time duration of this interval is equal to or less than the boosting time. This mode ends in either of two cases, whichever is sooner: the value of $v_{Cr}(t)$ equals the output voltage, or the boosting interval ends. The equations of the state variables can be derived from the equivalent circuit as:

$$i_{Lr}(t) = \frac{r_1}{Z_r}\sin(\pi - \omega_r(t - t_0)) \tag{4}$$

$$v_{Cr}(t) = (nV_{IN} + V_{OUT}) + r_1\cos(\pi - \omega_r(t - t_0)), \tag{5}$$

$$r_1 = nV_{IN} + V_{OUT} - v_{Cr}(t_0), \tag{6}$$

where $Z_r = \sqrt{L_r/C_r}$ is the characteristic impedance of the resonant tank, and $\omega_r = 1/\sqrt{L_rC_r}$ is the resonant angular frequency.

Mode II [$t_1' < t \leq t_1$] (remaining part of the boosting interval, if applicable): This mode has a probability of occurrence based on the operation scenario of the converter, as will be shown below. The equivalent circuit is shown in Figure 6b. The resonant capacitor voltage $v_{Cr}(t)$ remains constant at the V_{OUT} level until the end of the boosting interval at instant t_1. The main difference compared to Mode I is in the forward-biased state of D_2 where the anode–cathode voltage equals the corresponding forward voltage drop close to zero. The charging of the resonant inductor starts in the same positive direction but with a linear profile due to the short circuit formed through Q and D_2. The operation of the converter in this mode is similar to the conventional boost converter. Additionally, no power is exchanged between the load, and the input source provides L_r with the charging power. The equations of the state variables are as follows:

$$i_{Lr}(t) = i_{Lr}(t_1') + \frac{nV_{IN}}{L_r}(t - t_1') \tag{7}$$

$$v_{Cr}(t) = V_{OUT} \tag{8}$$

Mode III [$t_1 < t \leq t_2$] (first part of the discharge interval): It starts at turning off the switch Q as the boosting interval is over, while the top diode D_1 starts conducting. The stored energy in the resonant inductor during the boosting interval begins to transfer into the resonance capacitor, as shown in Figure 6c. The resonance capacitor continues charging from the previous mode, i.e., Mode I. It will be terminated when $v_{Cr}(t)$ reaches the output

voltage or the resonant current drops to zero. It has an occurrence probability based on the operating conditions. The state variable equations are defined as:

$$i_{Lr}(t) = \frac{r_2}{Z_r}\sin(\beta - \omega_r(t - t_1)), \tag{9}$$

$$v_{Cr}(t) = (nV_{IN}) + r_2\cos(\beta - \omega_r(t - t_1)), \tag{10}$$

$$r_2 = nV_{IN} - v_{Cr}(t_1), \tag{11}$$

where β is the initial angle of this interval.

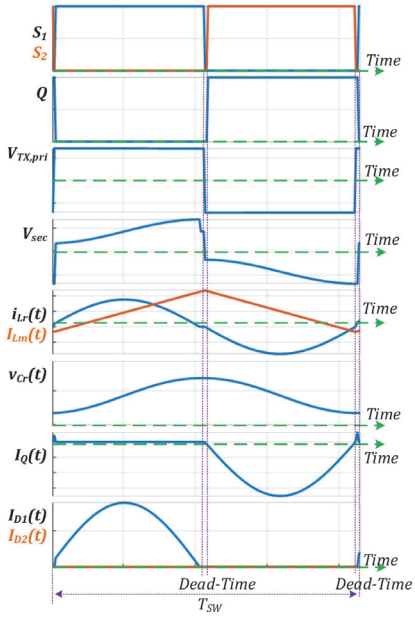


Figure 2. Steady-state waveform of the proposed converter under the nominal input voltage (*pure-SRC* conditions).

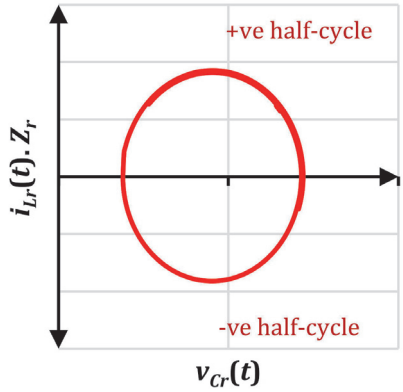


Figure 3. Trajectory curve of the converter state variables under the nominal input voltage (*pure-SRC* conditions).

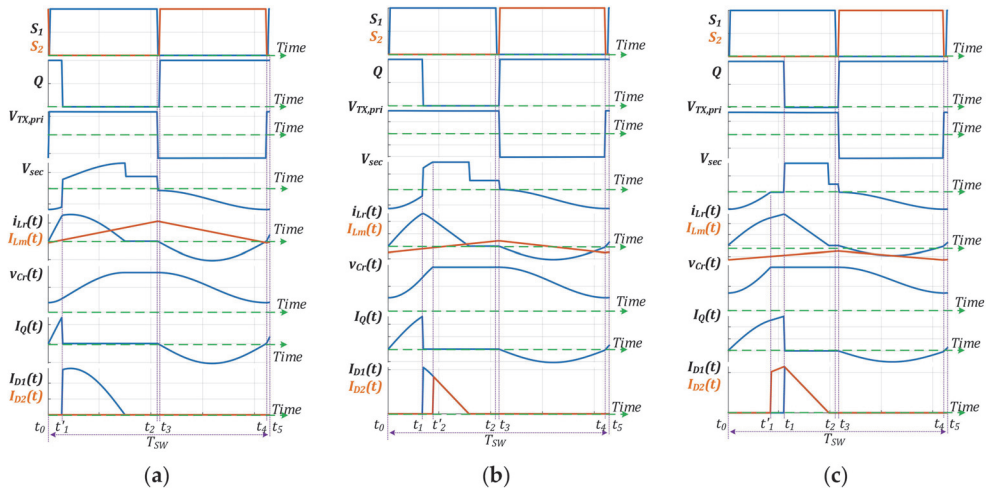


Figure 4. Steady-state waveforms of the proposed converter for three operation scenarios in the *boost-SRC* condition. (**a**) Scenario A: Forced half-resonance, (**b**) scenario B: Single-boosting mode, (**c**) scenario C: Double-boosting modes.

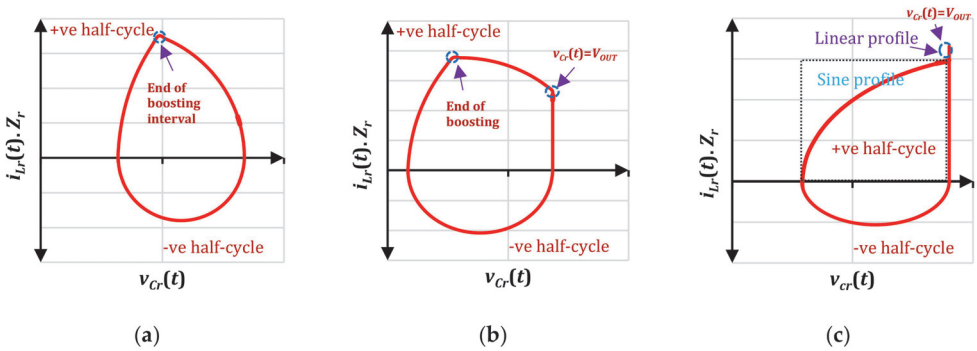


Figure 5. Trajectory curves of the converter state variables for the three possible scenarios in the *boost-SRC* conditions. (**a**) Scenario A, (**b**) scenario B, (**c**) scenario C.

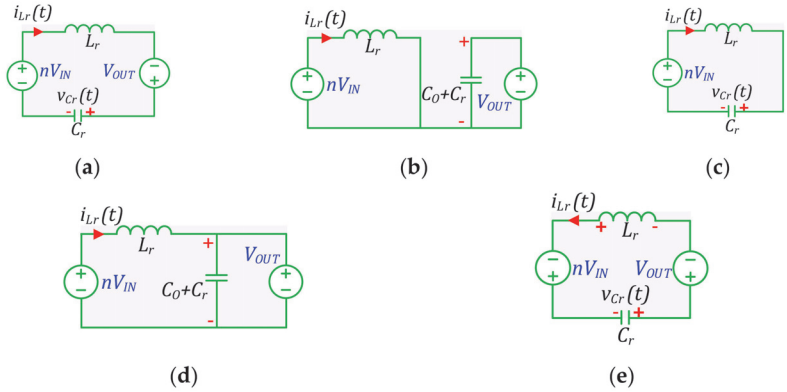


Figure 6. Equivalent circuits of the proposed converter in the *boost-SRC* conditions. (**a**) Mode I, (**b**) Mode II, (**c**) Mode III, (**d**) Mode IV, (**e**) Mode VI.

Mode IV [$t_2' < t \leq t_2$] (remaining part of the discharge interval): The capacitor voltage reaches the output voltage level at the boundary with Mode III. The equivalent circuit is shown in Figure 6d. The diode D_2 is conducting, and $v_{Cr}(t)$ remains constant at V_{OUT} until the next half-cycle. The discharging profile of the resonance current is linear. The converter works in the same way as a traditional boost converter, releasing accumulated energy into the load. The time domain expressions of the state variables can be given as:

$$i_{Lr}(t) = i_{Lr}(t_2') + \frac{nV_{IN} - V_{OUT}}{L_r}(t - t_2'), \tag{12}$$

$$v_{Cr}(t) = V_{OUT}. \tag{13}$$

Mode V [$t_2 < t \leq t_3$] (first dead time interval): This represents the first dead time interval between the gating signals of the primary switches in the same leg. Inserting the dead time avoids the possibility of a short circuit. The switches S_1 and S_4 are turned off. Therefore, all the primary switches are not conducting at the instant t_2. The magnetizing current reaches the peak value defined in (3). As stated earlier, I_m acts as a constant current source in the circuit, and it is reflected onto the primary side of the isolation transformer. It begins to flow through the parasitic output capacitance, C_{oss}, of S_1–S_4, where C_{oss} of $S_{1,4}$ is charging, and C_{oss} of $S_{2,3}$ is discharging. If the dead time is sufficient to discharge all parasitic capacitances fully, the switches $S_{2,3}$ will achieve a full soft-switching at zero voltage at the next turn-on, i.e., the beginning of Mode VI.

Mode VI [$t_3 < t \leq t_4$]: (half-resonance): The duration of this mode is nearly half of the switching period, as follows from the equivalent circuit given in Figure 6e. The switches S_2 and S_3 are synchronously turned on at the instant t_3. The switch Q is switched on as a synchronous rectifier to avoid conduction of its body diode to reduce the conduction losses. Both diodes of the rectifier cell are in the reverse biased state. The current of C_r is negative, and thus C_r begins to discharge in this mode. Additionally, between the input source and the load, there is a direct power transfer. This mode is similar to the conventional SRC operating close to the resonant frequency. The resonant current follows the sinusoidal shape, and its peak value i_{Lr_np} can be calculated using (14). The time domain equations of the state variables are given in (15) and (16).

$$i_{Lr\_np} = \frac{\Delta V_{Cr}}{2Z_r}, \tag{14}$$

$$i_{Lr}(t) = \frac{r_3}{Z_r}\sin(\pi - \omega_r(t - t_2)), \tag{15}$$

$$v_{Cr}(t) = nV_{IN} + r_3\cos(\pi - \omega_r(t - t_2)), \tag{16}$$

$$r_3 = -nV_{IN} + V_{OUT} - v_{Cr}(t_2). \tag{17}$$

Mode VII [$t_4 < t \leq t_5$] (second dead time interval): The end of the switching period and similar to Mode IV, but C_{oss} of $S_{1,4}$ is charging while that of $S_{2–3}$ is discharging. Consequently, $S_{1,4}$ will achieve zero-voltage switching (ZVS) at the beginning of the next mode, i.e., Mode I.

2.3. DC Voltage Gain Dependance on the Boosting Duty Cycle (D_b) for Each Operating Scenario

The part of the duty cycle of the switch Q that coincides with the positive half-cycle is used to boost the input voltage. It is designated here as D_b, where the time instant t_1 represents the boosting time interval, i.e., $D_b = t_1/T_{SW}$. The converter operation may include Modes I and II during one boosting interval. The maximum theoretical value of D_b is limited by half of the switching period as the switch Q operates with a duty cycle of over 0.5 for the synchronous rectification purpose. Table 1 summarizes the possible operation scenarios and defines the modes in each case. All three scenarios feature four common modes: I, V, VI, and VII.

Table 1. Converter operating scenarios in the *boost-SRC* conditions.

Description/Variable		Scenario		
		A	**B**	**C**
L_r is Charging in Boost Half-Cycle	Mode I	√	√	√
	Mode II	×	×	√
L_r is Discharging in Boost Half-Cycle	Mode III	√	√	×
	Mode IV	×	√	√
First Dead Time	Mode V	√	√	√
Negative Half-Cycle	Mode VI	√	√	√
Second Dead Time	Mode VII	√	√	√
ΔV_{Cr}		Equation (2)	$2nV_{IN}$	$2nV_{IN}$
V_{Cr}		Equation (21)	Equation (25)	Equation (27)
D_b		Equation (18)	Equation (22)	Equation (26)

2.3.1. Scenario A

If the value of ΔV_{Cr} defined by (2) equals or lower than $2nV_{IN}$, then the diode D_2 always remains reverse biased, and there is no need to find the value critical time, t_{cri}. Furthermore, the capacitor voltage of C_r does not reach the level of the output voltage, and t_{cri} is always larger than the term of $0.5T_{SW}$. The converter operation in this scenario is similar to that of the circuit in [16]. The duty cycle of the switch Q can be formulated as the following:

$$D_b = \frac{\cos^{-1}\left(\frac{R_2^2 - R_3^2 + V_{OUT}^2}{2R_2 V_{OUT}}\right)}{\omega_r T_{SW}}, \tag{18}$$

where R_2 and R_3 are radii of arcs on the state–space trajectory curves (Figure 5) defined as:

$$R_2 = 2nV_{IN} + \frac{\Delta V_{Cr}}{2} \tag{19}$$

$$R_3 = V_{OUT} - 2nV_{IN} + \frac{\Delta V_{Cr}}{2} \tag{20}$$

2.3.2. Scenario B

In this scenario, the capacitor voltage does not reach the output voltage at the instant t_1, i.e., $v_{Cr}(t_1) \leq V_{OUT}$, while applying the boosting interval. It features only Mode I when charging the resonance inductor and both Modes III and IV in the discharge operation. Consequently, it could be called a single-boosting case. The voltage across the inductor during the positive half-cycle is sketched in Figure 7a. Based on the volt–second balance of the inductor voltage during half of the switching period and assuming the linear behavior of the voltage during the time interval t_{d1} to simplify the analysis, the converter duty cycle can be expressed as:

$$D_b = \frac{\sin^{-1}\left(\frac{2\pi}{3} \cdot \sqrt{K\left(\frac{V_{OUT}^2}{n^2 V_{IN}^2} - \frac{V_{OUT}}{nV_{IN}}\right)}\right)}{\omega_r T_{SW}} \tag{21}$$

where the variable $K = \frac{2L_r P_{OUT}}{T_{SW} V_{OUT}^2}$ is used to simplify the equation.

When the boosting interval is over, the instantaneous value of the capacitor voltage, $v_{Cr}(t_1)$ can be calculated using (5) by substituting $t = t_1$, where $t_1 = D_b T_{SW}$. The additional

time, t_{d1}, is required during the discharge process of the resonance inductor for the capacitor to charge up to the output voltage:

$$t_{d1} = \frac{\cos^{-1}\left(1 - \frac{2nV_{IN} - v_{Cr}(t_1)}{nV_{IN}}\right)}{\omega_r}. \tag{22}$$

Therefore, the total time for $v_{Cr}(t) = V_{OUT}$ between the start of the positive half-cycle and the end of the boosting interval, which refers to the critical time, equals:

$$t_{cri} = t_1 + t_{d1} \tag{23}$$

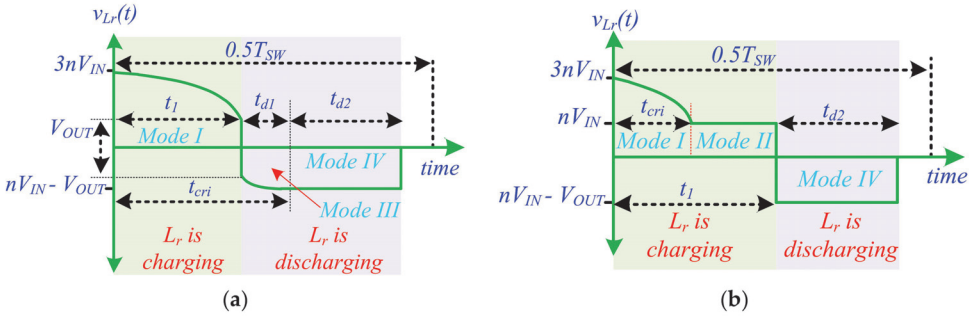


Figure 7. Timing diagram of the voltage across L_r in the positive half-cycle in the *boost-SRC* conditions for (**a**) scenario B and (**b**) scenario C.

2.3.3. Scenario C

The capacitor voltage charges up to the output voltage before the boosting interval ends, i.e., $t_{cri} < t_1$. Then, the diode D_2 conducts in the remaining part of the boosting interval. It could be called a double-boosting case as it includes both Modes I and II within the boosting interval. Consequently, Mode II will be followed only by Mode III when discharging the energy stored in L_r. The voltage across the resonance inductor during the positive half-cycle is plotted in Figure 7b. Applying the inductor volt–second balance during this half-cycle of the switching period yields:

$$D_b = \sqrt{K\left(\frac{V_{OUT}^2}{n^2V_{IN}^2} - \frac{V_{OUT}}{nV_{IN}}\right)} - \frac{1}{4} \tag{24}$$

The critical time can be given as:

$$t_{cri} \cong \frac{1.23}{\omega_r} \tag{25}$$

2.4. Transition between Operation Scenarios

Figure 8 shows the relationship between the critical time and the input voltage at various power levels of the converter. The range of the input voltage is adjusted to include only scenarios B and C, where the critical time is limited to half of the switching period ($T_{SW}/2$). It is evident from the figure that the critical time remains below or equal to $T_{SW}/2$ (2.06 µs) for the entire range of the input voltage for the operation scenario C (as in (25)). Meanwhile, in the region of scenario B, the capacitor voltage needs a longer time to charge up into the output voltage when the voltage is low until it reaches the boundary with scenario C. Additionally, the sketch clarifies the effect of the converter power on the voltage range for each scenario. The complete flowchart that shows how the converter operation

scenario could be defined is sketched in Figure 9. The operation scenario of the converter in the *boost-SRC* conditions is mainly dependent on the input voltage, converter power, and the resonant tank parameters.

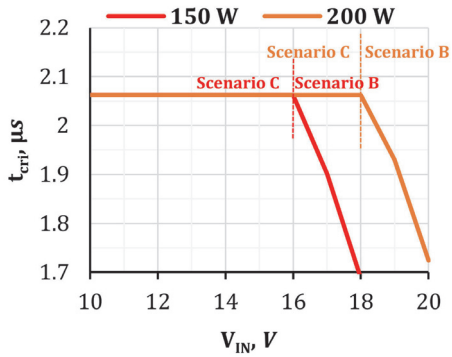


Figure 8. Dependence of t_{cri} on the input voltage at various power levels for scenarios B and C.

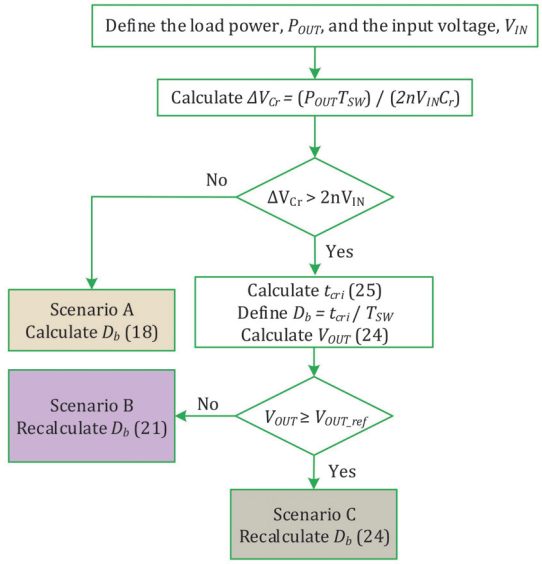


Figure 9. Flowchart of the operation scenario selection for the converter in the *boost-SRC* conditions.

3. Experimental Validation

3.1. Design Guidelines

3.1.1. Transformer

The transformer should be designed at the nominal input voltage, V_{IN_Nom}, which should correspond to the most probable operating point of the converter. Therefore, the turns ratio can be selected as in (26) to ensure the converter generates the desired output voltage at $D_b = 0$. Additionally, to reduce the copper loss and the proximity losses in the transformer windings, the Litz wire is preferably utilized where it has a large effective number of layers [9]. The magnetic material of the transformer core is the 3C95 ferrite with an ETD39 core type. This material has a low power loss per volume and is more suitable for low to medium switching frequency applications [18]. The number of turns in

the primary winding has to be optimized to avoid saturation of the core at the maximum input voltage (27). Additionally, the window area of the core should be taken into account when calculating the number of turns. After selecting the turn number of the primary winding, the secondary turns can be calculated based on the transformer turns ratio. The primary and secondary layers are preferably separated using an isolation material like Kapton tape to ensure high breakdown voltage of the isolation barrier [19]. This isolation material features a high temperature range as well as high strength [20].

$$n = \frac{V_{OUT}}{2V_{IN\_Nom}}, \tag{26}$$

$$B = \frac{V_{IN}}{2N_p A_c}, \tag{27}$$

where B is the peak-to-peak flux density in the core, N_p is the primary turns, and A_c is the effective cross-section area of the core. The magnetizing inductance shall be dimensioned so that the magnetizing current can fully charge and discharge the parasitic output capacitance of the primary semiconductors during the dead time [15] as:

$$L_m \leq \frac{n^2 T_{DT}}{8F_{SW}C_{oss}}, \tag{28}$$

where T_{DT} is dead time in the gating signals of the primary switches.

3.1.2. Resonance Tank Parameters

The resonance inductance affects the required duty cycle and the root mean square (RMS) value of the currents in the circuit. It needs to be optimized to minimize the losses at the nominal input voltage. The relation between the resonance inductance and the losses in the converter is depicted in Figure 10. The losses model of the semiconductors has been adopted from work in [21], while the core losses are estimated based on the improved generalized Steinmetz equation [22]. It is clear that when increasing the inductance, the losses in the circuit decrease. However, the leakage inductance should be low enough to ensure resonant tank operation with a discontinuous resonant current, i.e., a Q factor less than one. Next, C_r could be selected regarding the target resonance frequency and utilizing the value of L_r. The material of C_r should have a low series resistance and low temperature coefficient as well [13].

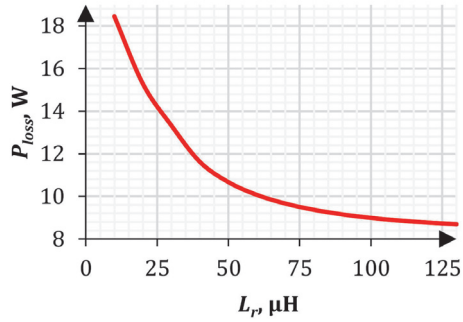


Figure 10. Dependence of the total power loss of the converter (P_{loss}) on the resonance inductance value.

3.2. Description of the Experimental Testbench

The rated power and the nominal input voltage of the designed converter are 300 W and 30 V, respectively. The turns ratio of the transformer equals six according to (26). The experimental setup photo is given in Figure 11, while the list of the parameters and

components utilized in the prototype is given in Table 2. An external inductor is wound to compensate for the low value of L_{lk} of the transformer. The resonance frequency of the converter is 92.3 kHz, which is close to the switching frequency to improve the converter efficiency. All efficiency measurements were taken with the Yokogawa WT1800 precision power analyzer, with the exception of the auxiliary power consumption. The control system is implemented utilizing the low-cost STM32F334 microprocessor.

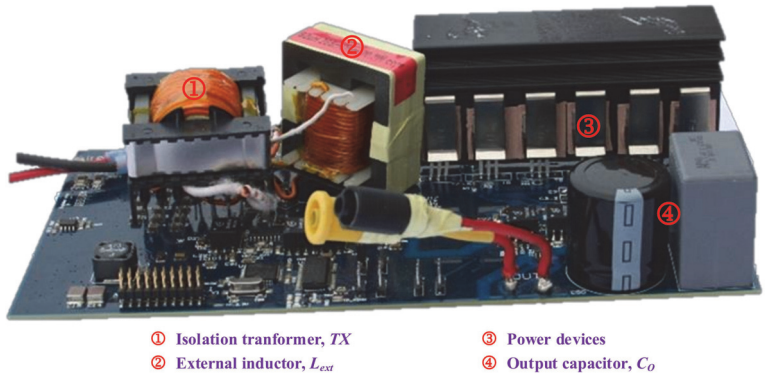


Figure 11. Experimental setup in the laboratory.

Table 2. Setup parameters and components.

Parameter	Symbol	Value
Input voltage range	V_{IN}	10:30 V
Input-side capacitor	C_{IN}	150 µF
Leakage inductance	L_{lk}	4 µH
External inductance	L_{ext}	92.5 µH
Magnetizing inductance	L_m	1 mH
Transformer core material	*TX*	Ferrite 3C95
Transformer core geometry		ETD39
Primary turns		9 (90 × 0.2)
Secondary turns		54 (90 × 0.1)
External inductor core material	L_{ext}	Ferrite 3C95
External inductor core geometry		E42
External inductor turns		33 (90 × 0.1)
External inductor core air gap		11 mm
Resonance capacitor	C_r	30 nF
Output-side capacitors	C_o	150 µF
Output voltage	V_{OUT}	350 V
Switching frequency	F_{SW}	95 kHz
Components	**Symbol**	**Part Number**
Primary side switches	$S_{1\text{-}4}$	FDMS86180
Bidirectional switch	Q	SCT2120AF
Output-side diodes	D_1, D_2	C3D02060E

3.3. DC Voltage Gain

Figure 12 shows the theoretical and experimental gain versus the boosting duty cycle D_b at different loading powers. The output voltage to input voltage ratio is referred to as the dc voltage gain, $G = V_{OUT}/V_{IN}$. The duty cycle represents only the boosting interval in the positive half-cycle of the switch Q. It can be noted that the two curves are approximately matched with a small deviation as the mathematical analysis is done for the lossless system. Furthermore, at the same dc voltage gain G, the power level influences the duty cycle value. Larger deviations between the theoretical and experimental gain curves

observed at lower powers can be explained by the effect of the parasitic capacitances of the output-side semiconductors.

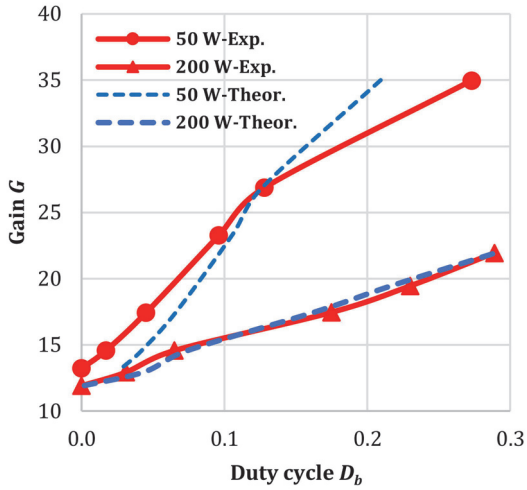


Figure 12. Theoretical and experimental dc voltage gain curves versus the boosting duty cycle D_b.

3.4. Measured Efficiency

The efficiency is measured in the *pure-SRC* conditions at 30 V and *boost-SRC* conditions at 25 V, as shown in Figure 13. The efficiency of *pure-SRC* is higher than at 25 V for most of the power levels due to negligible switching power losses. The peak efficiency of *pure-SRC* and 25 V equals 96.5% and 96%, respectively. The weighted California Energy Commission (CEC) efficiency equals 94.4% and 95.8% for the boost-SRC and pure-SRC conditions, respectively. At lower powers, the controllability is decreased as a smaller duty cycle D_b is needed to regulate the input voltage.

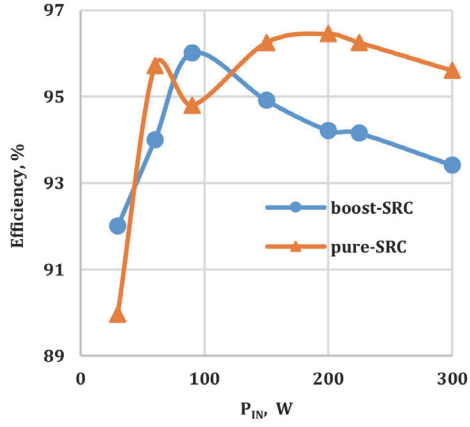


Figure 13. Measured efficiency of the proposed converter at the nominal input voltage of 30 V and in the boost-SRC at 25 V.

3.5. Comparison with the Existing Topology with an AC-Switch

The proposed topology is considered a modification of the baseline topology shown in Figure 14 [17]. The latter comprises two switches and two diodes to boost the input voltage,

implementing the ac-switch-based technique, i.e., using a bidirectional switch. The range of the input voltage that the two converters can regulate is measured in the laboratory, as shown in Figure 15a. It can be noted that the proposed topology covers a wider range than that of the topology in [17]. As can be observed from the figure, the proposed converter can regulate the input voltage and power in a wider range compared to the circuit based on the ac-switch. Next, the efficiency of both circuits was measured versus the power level, as shown in Figure 15b. It is worth noting that in pure-SRC conditions, all topologies work the same at the nominal voltage. The proposed topology provides slightly lower efficiency in the boost-SRC conditions at 25 V, which, however, is a justifiable disadvantage considering the improved converter regulation range.

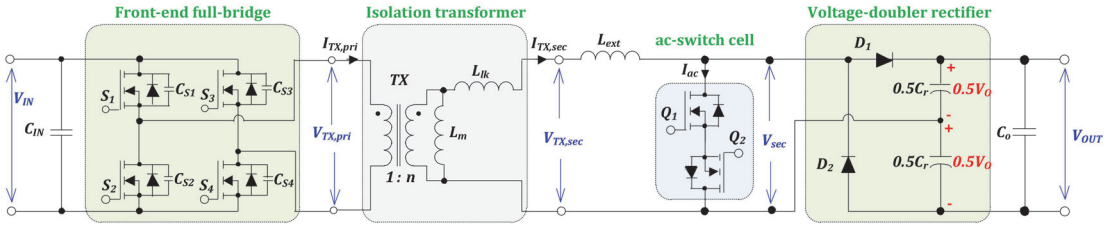


Figure 14. SRC configuration based on the ac-switch boosting technique [17].

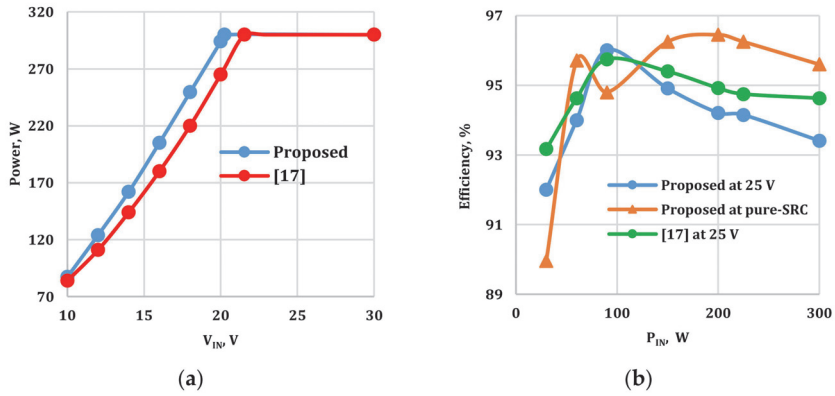


Figure 15. Comparison between the proposed topology and the topology in [17]: (**a**) Measured operating range and (**b**) measured efficiency.

3.6. Steady-State Waveforms

3.6.1. *Pure-SRC* Conditions

The experimental results for the trajectory curve and the steady-state waveforms are shown in Figures 16 and 17, respectively. The operating power of the converter was 200 W. The radius of the bottom half-circle in the state trajectory is 210 V, which refers to the peak-to-peak ripple of the resonant capacitor voltage, and the theoretical value of ΔV_{Cr} equals 198.5 V. In the negative half-cycle, the secondary winding (resonant) current follows the half-wave sinusoidal shape with a peak value of 1.85 A. The resonant capacitor discharges from the value of 285 V down to 75 V at the end of this half-cycle. At the end of the positive half-cycle, the converter operates in the freewheeling condition for a short time.

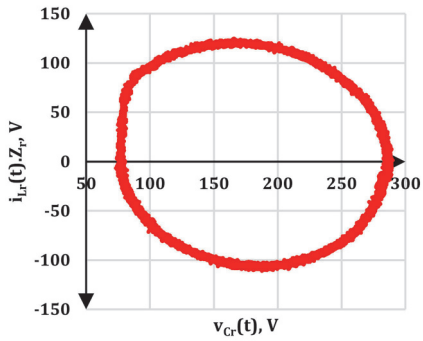


Figure 16. Measured state–space trajectory curve in the *pure-SRC* conditions.

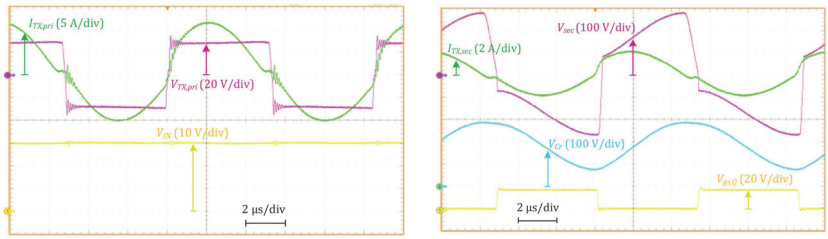


Figure 17. Steady-state waveforms of the converter in the *pure-SRC* conditions: (**a**) At the input and (**b**) output sides.

3.6.2. *Boost-SRC*, Scenario A

The trajectory curve and the steady-state waveforms are shown in Figure 18. In this case, the input voltage and the converter power equal 25 V and 200 W, respectively. The measured value of ΔV_{Cr} is 232 V, which matches the theoretical prediction of 234 V calculated from (2). The boosting duty cycle D_b equals 0.055. The value of the secondary current, $I_{TX,sec}$, at the end of the boosting interval is 2.8 A. The converter operation corresponds to the theoretical analysis. As the resonant current decreases to zero, parasitic voltage oscillations are generated by parasitic capacitances of the output-side semiconductors, but this has little effect on the converter's main operating principle.

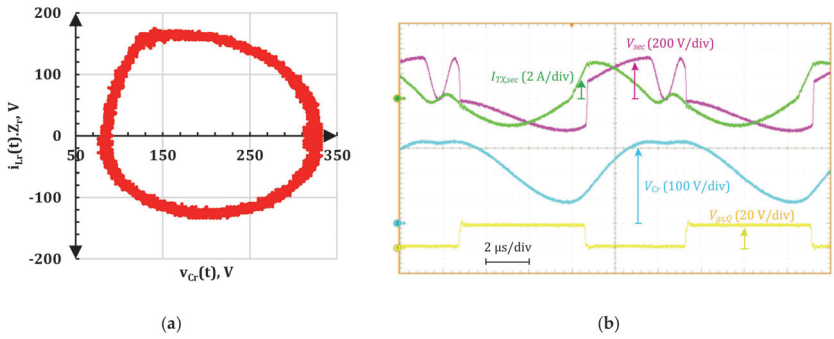
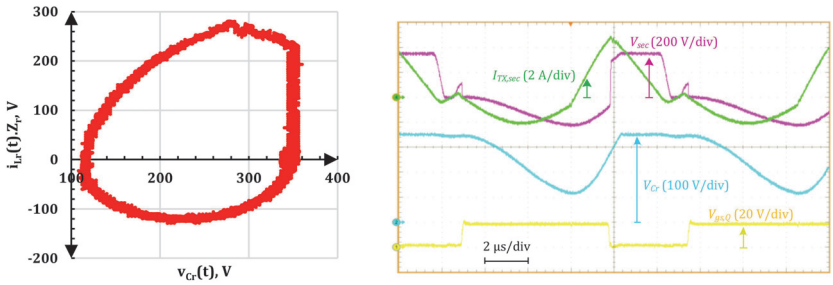


Figure 18. Experimental waveform of the proposed converter for scenario A: (**a**) Trajectory curve and (**b**) steady-state waveforms.

3.6.3. *Boost-SRC*, Scenario B

During this case, the input voltage and the power level are 20 V and 200 W, respectively. The experimental results for the trajectory curve and the steady-state waveforms are shown in Figure 19. The boosting duty cycle D_b equals 0.15. It is clear that the converter has a single-boosting mode as the capacitor continues charging while the resonance inductor is discharging in the positive half-cycle. Further, the capacitor voltage in the negative half-cycle starts discharging from the output voltage of 350 V down to 105 V at the end of the half-cycle. This change in the voltage V_{Cr} represents the peak-to-peak ripple, which matches the theoretical value at $2nV_{IN}$, i.e., 240 V. During the boosting interval, the inductor current charges according to the sinusoidal law up to approximately 5 A, then it begins to discharge until the resonant current drops to zero. It is worth mentioning that the resonant capacitor voltage reaches the output voltage level soon after the boosting interval is finished and remains unchanged till the end of the half-cycle.

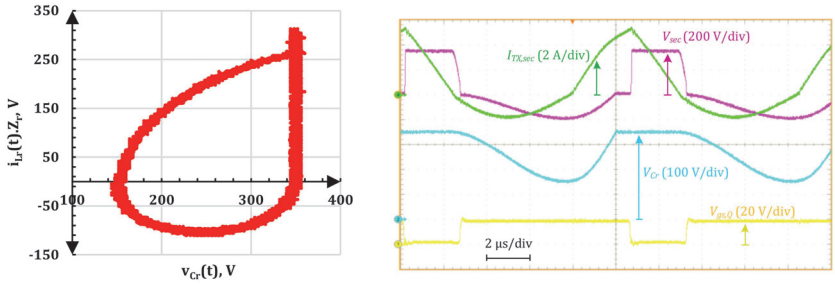


(**a**) (**b**)

Figure 19. Experimental waveform of the proposed converter for scenario B: (**a**) Trajectory curve and (**b**) steady-state waveforms.

3.6.4. *Boost-SRC*, Scenario C

During this case, the input voltage is set to 17 V, the converter power equals 200 W, while the boosting duty cycle D_b equals 0.15. The experimental result of the trajectory curve is shown in Figure 20a, and the obtained shape matches the theoretical one in Figure 5c. The capacitor voltage reaches the output voltage before ending the boosting interval, as shown in Figure 20b. The secondary winding current changes according to the sinusoidal law before the instant when $v_{Cr}(t) = V_{OUT}$, and linearly after that. The theoretical and measured values of ΔV_{Cr} are 204 V and 205 V, respectively. The two values are well matched, which confirms the validity of the circuit analysis in this case.



(**a**) (**b**)

Figure 20. Experimental waveform of the proposed converter for scenario C: (**a**) Trajectory curve, and (**b**) steady-state waveforms.

A simple closed-loop control system is designed to generate the duty cycle that will regulate the output voltage at its reference point, as shown in Figure 21. When a maximum is hit, the anti-windup feedback limits the input of the integrator, preventing a significant value of integrating action. The proportional and integral gains of the proportional-integral (PI) regulator are 0.23 and 0.001, respectively. The system is tested in two conditions to ensure the robustness of the designed regulator. First, the load resistance is changed in a step from 1000 Ω to 500 Ω, i.e., the power is changed from 122.5 W to 245 W. The output voltage remains constant at 350 V, as shown in Figure 22a. The input voltage during this test equals 25 V, and the input current increases from 5.5 A to 11.3 A, corresponding to the load step. Additionally, ΔV_{Cr} changes with the power level, which agrees with the theoretical prediction (2).

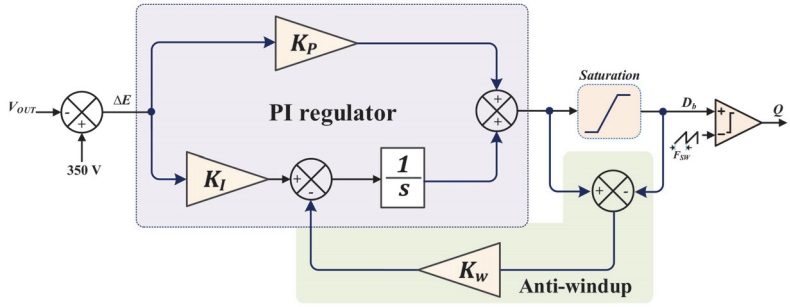
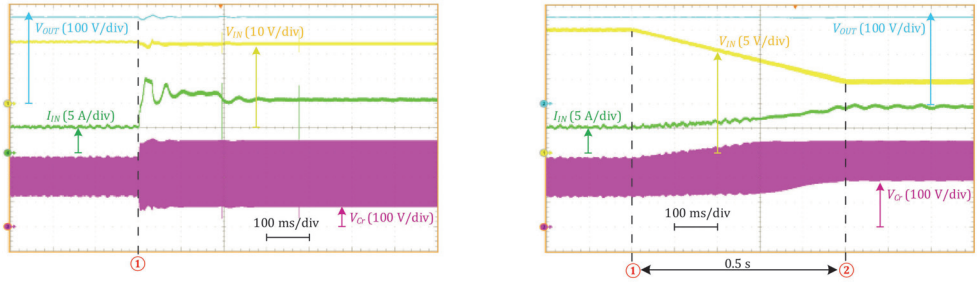


Figure 21. Block diagram of the closed-loop system using the PI regulator with an anti-windup strategy.



(**a**) (**b**)

Figure 22. The converter response to (**a**) load step change and (**b**) the input voltage ramp.

The next test is done by ramping the input voltage from 25 V down to 15 V within 0.5 s, while the load resistance equals 1000 Ω. The response of the converter output voltage is shown in Figure 22b. The converter operates in the *boost-SRC* condition and switches between all three operation scenarios during this input voltage change.

The resonant capacitor voltage stress constraint on the output voltage is a significant advantage of the proposed converter. It is known that resonant capacitors are prone to failure in galvanically isolated dc-dc converters [23]. In other existing topologies, including the single form [17], the resonant capacitor could experience much higher voltage stress during transients due to resonant current overshoots, which is avoided in the proposed converter.

4. Conclusions

The paper has introduced a new topology of the series resonant dc-dc converter with galvanic isolation and discontinuous resonant current. This topology utilizes a novel boosting rectifier cell with one MOSFET, two diodes, and two capacitors at the high voltage

side. It employs the converter resonant inductor as a boost inductor for voltage boost. Compared to its counterparts based on a voltage doubler rectifier, this boosting cell reduces the number of semiconductor components and clamps the resonant capacitor voltage to the maximum output voltage. The latter feature ensures safe converter operation under any regulation transients when connected to a stable dc microgrid, but it provides slightly lower efficiency compared to the closest existing SRC-based topology with an ac-switch. Nevertheless, the proposed converter can achieve the soft switching feature, and the maximum efficiency of the converter was 96.5%. The obtained features enable using the proposed converter in distributed generation applications where it needs to operate in a wide range of input voltage and power.

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Nomenclature

PV	Photovoltaic
SRC	Series resonant converter
ZVS	Zero voltage switching
LLC	Inductor-inductor-capacitor resonant converter
MOSFET	Metal oxide semiconductor field-effect transistor
C_r	Resonant capacitance (F)
F_r	Resonant frequency (Hz)
F_{SW}	Switching frequency (Hz)
L_r	Resonant inductance (H)
L_{lk}	Leakage inductance (H)
L_{ext}	External inductance (H)
V_{Cr}	The average voltage of the resonant capacitor (V)
V_{OUT}	Output voltage (V)
L_m	The magnetizing inductance of the transformer (H)
n	Turns ratio of the transformer
C_{oss}	Parasitic output capacitance of the input-side bridge semiconductors
D_b	Cumulative boosting duty cycle
T_{SW}	Switching period (s)
P_{OUT}	Output power (W)
ΔV_{Cr}	The peak-to-peak ripple of the resonant capacitor voltage
V_{IN}	Input voltage (V)
C_O	Output capacitance (F)
Z_r	Resonant impedance (Ω)
ZCS	Zero current switching
ω_r	Angular resonant frequency (rad/s)
β	Initial angle (rad)

DCM	Discontinuous conduction mode
G	Normalized dc voltage gain
P_{IN}	Input power (W)
B	Peak-to-peak flux density of the transformer (Weber/m^2)
N_p	Number of the primary winding turns
A_c	Effective core area (m^2)
T_{DT}	Dead-time between the two MOSFETs in the input-side bridge (s)
t_{cri}	Critical time to charge the resonance capacitor into the output voltage (s)
V_{OUT_ref}	Reference of the output voltage

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Effect of Mission Profile Resolution on Photovoltaic Energy Yield Prediction in Python and MATLAB

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***Abstract*—This paper studies the effect of the resolution of the mission profile, i.e., solar irradiance and ambient temperature, on prediction accuracy of the photovoltaic (PV) module energy yield. The case study considers integration of a PV module into a DC microgrid (MG). The mission profile that corresponds to North Denmark is utilized as it exemplifies a climate environment with cloudy days with fluctuating solar irradiance. The paper considers the long-term prediction of the PV output power for one year. Mission profile resolutions of 1 s, 10 s, 30 s, 1 min, 5 min, and 15 min are considered. The interface converter between the PV module and DC MG is based on the series resonant converter (SRC) that has buck-boost functionality, which results in non-smooth efficiency dependence on the input voltage and power. The algorithm predicting the energy yield has been carried out in the Python and MATLAB environments. The performance of the two environments is compared.**

***Index Terms*—Mission profile, Photovoltaic (PV), energy yield prediction, DC microgrid**

I. Introduction

Recently, global trends move towards increasing the deployment of renewable energy in most of life activities. There is an evident trend of energy electrification end-use in all sectors, including even heating. One of the main reasons behind these trends is to avoid the problems of climate change that threaten our planet. Photovoltaic (PV) modules are widely used as renewable energy resources to harness the solar energy and convert it into electricity. The development of PV technologies provides cost-effective solutions in different markets. In 2030, the global electricity generated by solar photovoltaics could grow up to 13% according to the IRENA report [1], and the expected electricity price for residential PV systems in the USA is 0.05 USD/kWh [2].

It is well known that the power generated from PV modules is variable and is subjected to environmental conditions. Predicting the energy production of the PV systems based on the annual mission profile from the previous year, allows the decision-maker to take an overview of the generation capacity versus the required one. Besides, the prediction of the solar energy production improves grid flexibility [3]. Furthermore, the predictive maintenance strategy could be set according to the low power profile in such days [4].

With the growth of integration of renewable energy into utility services, the reliability issue of the installed PV systems has risen as a big concern. The PV output power is mainly affected by the mission profile of the incident irradiance and the ambient temperature. To study the actual behavior of the PV system from the point of reliability prediction and system-level availability, or to predict the energy yield for a certain long-time horizon, the mission profile of the operating conditions is required. The time step, i.e., resolution, of the mission profile dataset depends on some factors such as implementation cost, dataset capacity, and the installation environment in some cases. To gather the mission profile at a high resolution, a powerful data logger is necessary to rapidly record the environmental data at an acceptable precision, which is deemed an expensive option [5]. The utilized resolution in the literature work includes a variety of values in the range from 1 second into 1 hour for long-term studies, i.e., one-year [6]- [7]. The impact of the mission profile resolution on the reliability prediction and lifetime consumption for PV inverter semiconductors has been investigated in [8]. The results of this work reported that the mission profile resolution affects strongly the reliability prediction, especially in the cloudy environment, and an overestimation of the PV inverter lifetime could result from low resolution of the mission profile. The work in [9] proposes a variable dc-link operation for the buck-boost converter with the PV system, and it takes into account the change of the PV module series resistance with the temperature. In the latter work, the energy yield prediction algorithm is investigated only at a 1 min resolution to predict the annual energy yield.

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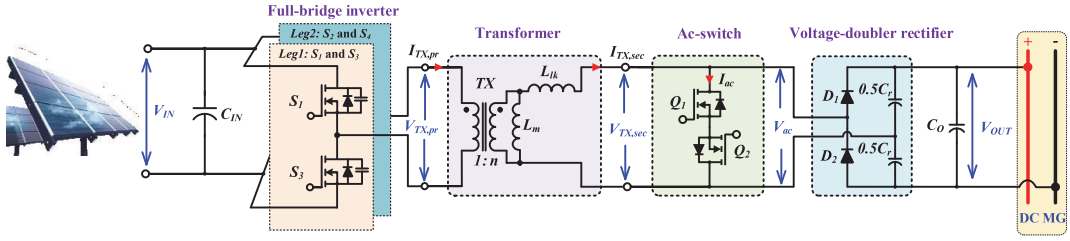


Fig. 1: A residential PV system including an SRC-based converter coupling the PV module to the DC MG.

This paper aims to answer the question of how the mission profile resolution can affect the accuracy of the energy yield prediction for a PV module connected to the DC MG. Different mission profile resolutions are considered for the same PV module and the interface converter parameters. In this paper, the energy yield prediction algorithm is implemented using Python and MATLAB software to compare the execution speed.

II. Description of the Studied System

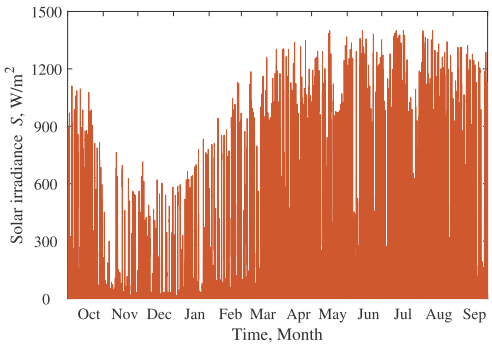
The studied system considers feeding the power generated by the PV system to the DC microgrid. One PV module is used during this study to match the designed converter prototype. The considered PV module is 60-cell Jink Solar JKM300M-60B with monocrystalline silicon technology. The complete structure of the studied system is provided in Fig. 1, while the system parameters are listed in Table I.

A. Mission profile

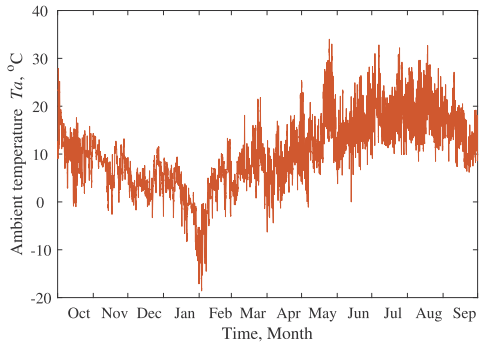
The PV energy production is mainly affected by the mission profile of solar irradiance and ambient temperature. As a result, the day with more clouds leads to fluctuations in the PV power along with the daylight time. To investigate the effect of mission profile resolution on the energy yield prediction, the mission profile recorded in Northern Denmark shown in Fig. 2

TABLE I: SRC parameters in the studied residential PV system.

Parameter	Symbol	Value
Input voltage range	V_{IN}	10:50 V
Input capacitance	C_{IN}	150 μF
Transformer turns ratio	n	5.5
Resonant inductance	L_{lk}	106 μH
Magnetizing inductance	L_m	1.46 mH
Resonant capacitance	C_r	30 nF
Switching frequency	F_{sw}	95 kHz
Output capacitance	C_O	150 μF
Output voltage	V_{OUT}	350 V



(a)



(b)

Fig. 2: Annual mission profile for Aalborg, Denmark: a) solar irradiance and b) ambient temperature.

is used. Notably, this location is considered a soft environment with highly variable solar irradiance mission profile compared to the location like Arizona in the USA, which represents a harsh environment as the ambient temperature is high. The average level of solar irradiance is relatively low from November to February. The same distribution profile can be noted for the ambient temperature.

B. DC-DC converter based on series resonant converter

SRC is considered a promising solution to overcome the wide-range variations of the input voltage [10]- [14]. As

shown in Fig. 1, SRC has a high switching frequency full-bridge inverter on the input side. The two switches of the front-end bridge must not be switched ON simultaneously to avoid the supply short-circuit, so a small dead-time is inserted in the modulation sequence. This converter features soft-switching characteristics utilizing the magnetizing current during the dead-time interval to charge/discharge the parasitic output capacitance of the bridge MOSFETs. To achieve that, the switching frequency must be 5-10% lower than the resonant frequency to attain soft-switching, i.e., high efficiency [15]. Also, it has the buck-boost functionality with the same power stage when using different modulation techniques. This converter provides galvanic isolation utilizing the high step-up transformer, *TX*. The ac-switch on the output side is a bidirectional switch that could be driven to boost the input voltage [16]. When the studied converter operates in the discontinuous conduction mode, the voltage doubler diodes could be turned off at zero current and achieve high efficiency. More details about the studied converter can be found in [16].

III. Energy Yield Prediction

The energy yield prediction algorithm starts with reading the PV mission profile with a certain resolution as shown in Fig. 3. Then the ambient temperature, T_a, is employed to determine the cell temperature of the module, T_c, based on a first-order low-pass filter as below:

$$T_c = \left(T_a + \frac{T_{NOCT}}{T_{a(NOCT)}}.s \right) . \frac{1}{1+s\tau} \tag{1}$$

where, T_{NOCT} is the nominal operating cell temperature, $T_{a(NOCT)}$ is T_a at the nominal operating cell temperature, τ is the time constant of the low-pass filter, and s represents the Laplace operator.

It is worth to mention that the thermal response of the PV cell effect on the time response of the cell temperature with the ambient temperature change, and therefore the prediction of the energy yield. To model of the PV module, the single-diode model is utilized with the series resistance, R_s and the shunt resistance, R_{sh} as the parasitic element of the PV module. Here, during the modeling of PV module, R_s is not considered fixed, but it changes with the cell temperature as below [17]:

$$R_s = R_{s(STC)} . (1 + k_{rs} (T_c - T_{STC})) \tag{2}$$

where, $R_{s(STC)}$ is R_s at the standard test condition, and k_{rs} is the experimental thermal coefficient.

Using the methodology from [9], it is possible to define the annual voltage and current profiles of the PV interface converter. Next, an interpolation of the converter efficiency versus converter input voltage and current can be derived from the experimental measurements of the SRC converter. This contour plot of SRC efficiency is given in Fig. 4. Based on the maximum power fed from the PV module, the converter output power, P_{OUT}, can be calculated using the experimental efficiency interpolation.Then, the energy yield prediction, E, during an arbitrary interval t_x could be calculated as:

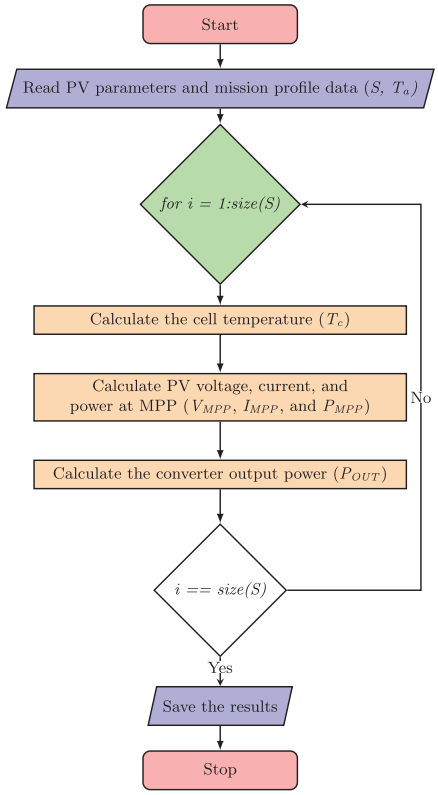


Fig. 3: Flowchart of the PV energy yield prediction.

$$E = \int_0^{t_x} P_{OUT}(t)dt \tag{3}$$

More details about the prediction algorithm of the PV energy yield based on PV module datasheet parameters could be found in [9].

IV. Results and Discussion

The solar irradiance for one day out of the yearly mission profile is given in Fig. 5 for two cases, clear and cloudy, at different resolutions. It is clear that the resolution of the solar irradiance profile has negligible influence on the clear-day mission profile, where the solar irradiance has a low dynamic change. On the other hand, the dynamic change in solar irradiance, especially for the fast cloudy environment, differs a little from the mission profile resolution.

The cumulative energy of the PV module during one year is summarized in Table II for different resolutions. The total energy (in kWh) of the PV module is approximately the same for all considered resolutions. The difference between the estimated energy yields is less than 0.5 %. This effect could be explained by analyzing the annual output power profile using

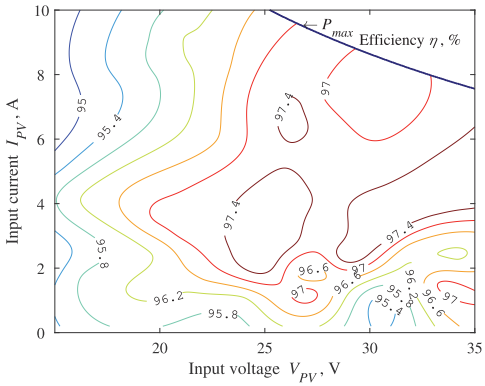


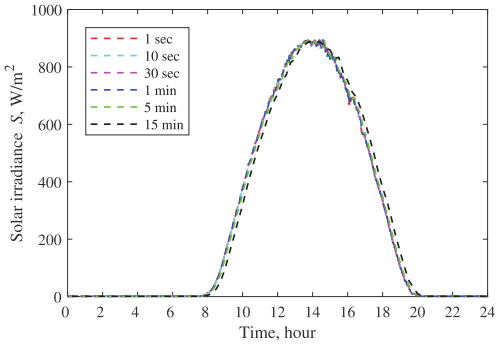
Fig. 4: Contour plot of the SRC efficiency versus the converter input voltage and current based on experimental data and thin plate spline interpolation.

rainflow counting algorithm. Fig. 6 shows that there are almost no power cycles above 30 W and they appear mostly in the output power range between 50 W and 250 W. Moreover, the duration of these cycles is mostly shorter than 30 s as shown in Fig. 7. This proves that the high variability in the annual solar irradiance does not impose a high requirement on the mission profile resolution when the energy yield needs to be predicted. However, it is essential in other research topics, like estimation of wear-out failure probability of semiconductor components [8].

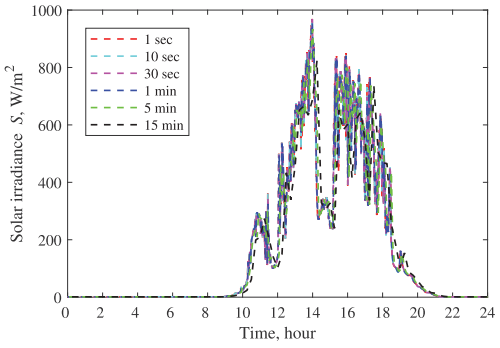
At the end, we have compared the performance of two typical softwares used for solving this type of computational problems: Python and MATLAB. The Python libraries used during the implementation include *numpy*, *scipy*, and *pandas*. They provide very high execution speed due to their implementation in C programming language. The bar diagram in Fig. 8 shows the computational time for both the Python and MATLAB scripts for different mission profile resolutions. The algorithm is running on a personal computer employing Intel(R) Core(TM) i5-8265U processor operating at 1.60 GHz and 16 GB of RAM. Also, the calculated time does not include the time of saving the results into the format of comma separated values (CSV), which was used for storing large datasets. It is clear that Python environment with C-based libraries provides from two to over four times the calculation speed improvement over that in MATLAB.

TABLE II: Energy yield prediction for different resolutions.

Resolution	**1 s**	**10 s**	**30 s**	**1 min**	**5 min**	**15 min**
***E*, kWh**	314.0	314.52	314.54	314.57	314.75	315.12



(a)



(b)

Fig. 5: Mission profile of Aalborg at different resolutions in: a) clear day and b) cloudy day.

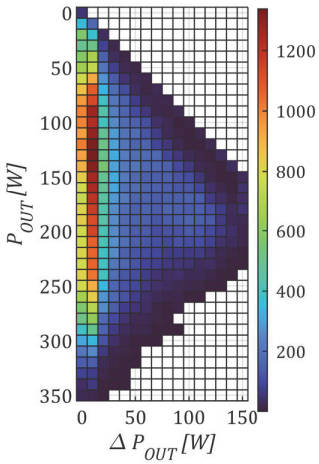


Fig. 6: Results of rainflow counting algorithm for the average output power versus output power cycle swing.

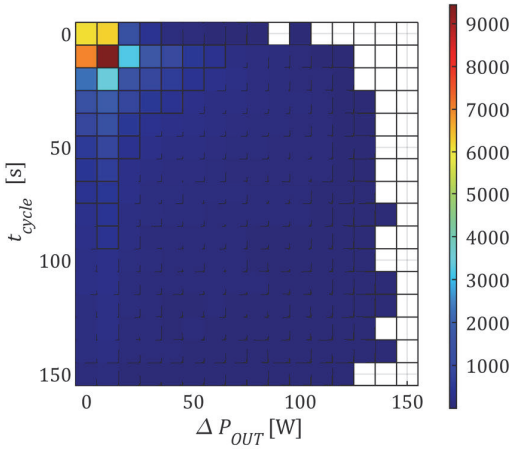


Fig. 7: Results of rainflow counting algorithm for the the output power cycle duration versus its swing.

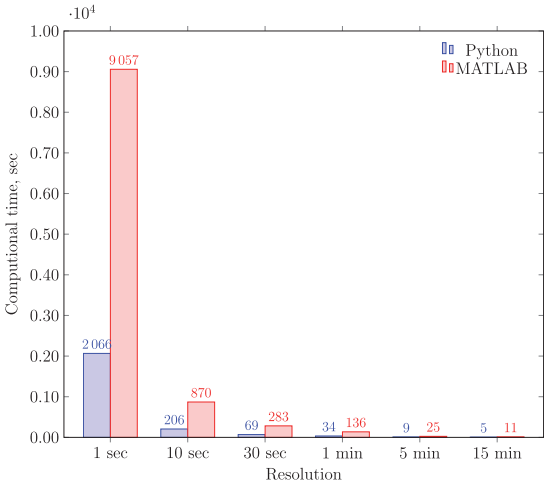


Fig. 8: Computational time of Python environment versus MATLAB at different mission profile resolutions.

V. Conclusion

The paper has discussed the effect of mission profile resolution on the annual prediction of the energy produced from the PV module connected to the DC microgrid via a buck-boost galvanically isolated dc-dc converter. The original annual mission profile comprised of the solar irradiance and ambient temperature recorded in Aalborg, Denmark, with a resolution of 1 s was downsampled to resolutions of 10 s, 30 s, 1 min, 5 min, and 15 min. The results show that the energy yield prediction does not require resolutions below 15 min. In addition, the paper shows that using the Python environment with popular C-based libraries could save computational time by 55-80 % versus the MATLAB environment.

Acknowledgment

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Reliability Evaluation of Isolated Buck-Boost DC-DC Series Resonant Converter

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ABSTRACT This paper investigates the reliability of an isolated buck-boost DC-DC converter (IBBC) based on the configuration of a series resonant converter (SRC). Two approaches are employed to predict the IBBC reliability, which are based on the MIL-HDBK-217F handbook and FIDES guide. The latter approach can take into account how the failure rate of the converter components based on the physics of failure is influenced by a varying yearly mission profile. To do this, the thermal loading of each IBBC component is obtained, taking into account the photovoltaic (PV) mission profile of the solar irradiance and ambient temperature. In such a case, the PV module is operating at the maximum power point (MPP) and the IBBC transfers this power into the DC microgrid (MG). Second, the component-level failure rate is calculated with both reliability assessment approaches, to evaluate the converter-level failure rate. Therefore, the converter reliability can be defined while taking the serial reliability connection of the converter components into account. The reliability analysis is carried out using a cloud Python engine installed and running in a Google Colaboratory notebook. The results indicate that the primary semiconductors are the most vulnerable component in the IBBC. The B_{10} lifetime of the case-study IBBC calculated using the MIL-HDBK-217F and FIDES approaches is 14.80 and 23.20 years, respectively. This indicates that, when compared to the methodology from the MIL-HDBK-217F handbook, the approach from the FIDES guide can provide a more accurate prediction for the IBBC lifespan considering the real field mission profile.

INDEX TERMS Isolated DC-DC converter, series resonant converter (SRC), reliability, lifetime, MIL-HDBK-217F handbook, FIDES approach.

I. INTRODUCTION

Nowadays, power electronics represent a major challenge in solar energy systems since they are more prone to failure, up to 66 % [1], and consequently have lower lifetime compared to the PV module lifetime, which could reach up to 25 years. With the significant spread of renewable solar energy worldwide to preserve the environment and mitigate climate changes, the research community has carefully considered the reliability of power electronic converters at the design phase (i.e., design for reliability (DFR)). In addition, it is important to continue assessment and monitoring of the reliability of the power converter over time to ensure that the system works successfully [2].

Generally speaking, DC-DC converters are widespread in different applications such as renewable energy systems, data centers, electric vehicles, home appliances, and aircraft [3]. Their reliability should be emphasized well in different operating conditions and applications. The reliability of the three-phase interleaved boost converter is analyzed in [4], and the results show that soft-switching improves the converter reliability compared to hard-switching. In addition, the series resistance of the main switch or the output capacitor in the conventional boost converter degrades the reliability performance of the converter [5]. In [6], a reliability assessment approach based on Markov chain modeling proves that the two-stage boost converter with half-power operation has high

reliability with the single-stage conventional boost converter operating at full power.

For the isolated DC-DC converters with a single switch (such as Flyback, Forward, Cuk, SEPIC, and Zeta topology) or multiple switch (such as Full-bridge, Half-bridge, and Push-pull), their reliability have been investigated using the MIL-HDBK-217F handbook in [7]. But, the MIL-HDBK-217F handbook has been in development since 1961, and the most recent version was released in 1995, making it an outdated reliability guide. It also calculates component failure rates without considering process factors such as manufacturing or software. The used Markov model disregards the converter operation mission profile, resulting in an underestimation of the converter lifespan. It is worth noting that the PV system is turned off at night, and the mission profile duration depends on the PV mission profile. The reliability of the converter due to fluctuations in photovoltaic energy has also been discussed in [8].

The isolated series resonant converter (SRC) emerges as a most promising isolated DC-DC converter to regulate the wide range variation in input voltage for PV applications [9] as i) it has direct power transfer to the load, ii) good transformer utilization, and iii) soft-switching features. Moreover, it can work at a fixed-switching frequency while retaining the soft-switching through the magnetizing current of the isolation transformer. According to industrial statistics, the primary semiconductors, followed by the resonant capacitor, are the most prone components in the SRC/LLC converters [10]. The short-circuit faults are dominant in the primary semiconductor faults, while the resonant capacitor faults occur in the form of an open-circuits, which causes the secondary side power to be unplugged from the load. The reliability in the isolated DC-DC converters such as LLC, SRC, dual active bridge, and phase-shift converter when using the Si and GaN power devices on the high voltage side is investigated for a one-day mission profile in [11]. In that study, the designed SRC operates at a variable switching frequency, and the failure rate of the resonant capacitor and isolation transformer has not been addressed. Furthermore, there is a trade-off between the selection of resonant tank parameters to improve the reliability of the SRC, where the resonant capacitor tank should have a high capacitance value and a small inductance value at the given resonant frequency, as reported in [12]. On the other hand, such a design can seriously penalize the efficiency of the SRC-based IBBC [13].

In this paper, the reliability of IBBC based on the SRC will be explored, taking into account a real annual PV mission profile recorded in Aalborg, Denmark. To analyze component-level reliability, the failure rate for the primary and secondary IBBC semiconductors is assessed in addition to the isolation transformer and resonant capacitor. To consider the yearly mission profile of PV, the approach from the FIDES guide will be used and compared to the approach from the MIL-HDBK-217F handbook that does not consider this. By analyzing the failure rate of each IBBC component, the most prone component can be identified and replaced/redesigned during the design phase. It is the first time that the failure rates of all power components of the SRC-based IBBC have been examined for PV applications. The rest of the paper is as follows: Section II covers details of the mission profile utilized, in addition to the basic operation of SRC-based IBBC. Section III addresses the thermal modeling for the primary and secondary semiconductors, the isolation transformer, and capacitors, which is regarded as the most important step in the reliability prediction. Then, Section IV discusses the reliability mathematical models for both MIL-HDBK-217F and FIDES based approaches in each component category, and the system-level reliability of the power electronic converter is also evaluated. The findings of the reliability analysis are given and discussed in Section V. Finally, the conclusions and future work of the paper are drawn in Section VI.

II. DESCRIPTION OF THE STUDIED SYSTEM

The case study for the SRC-based IBBC is aimed at a PV module-level application in the DC microgrid (MG). The entire configuration of the investigated system is shown in Fig. 1, while the parameters of the PV module based on Jinko Solar JKM300M-60B are adopted from the work [14]. The PV module operates at the maximum power point (MPP) by adopting the perturb and observe (P&O) technique due to its simplicity. The MPP tracking is achieved by phase shift modulation at the input side in the buck mode, or pulse-width modulation at the output side in the boost mode [15]. The voltage of DC MG is assumed to be fixed and ripple-free during the analysis in this paper. Additionally, the leakage inductance of the isolation transformer incorporates the resonant inductance of the resonant tank.

A. UTILIZED YEARLY MISSION PROFILE

It is widely known that PV power is influenced by the weather conditions of solar irradiance (S) and ambient temperature (T_a), which will reflect the mission profile for the reliability assessment. The presence of more clouds on a given day might cause variations in the PV power throughout the day. Consequently, the thermal stress of the PV converter components would be strongly affected [16]. The considered mission profile is recorded for Northern Denmark (Aalborg) with a resolution of one second and a total of 31,863,123 points per year, as shown in Fig. 2. It is clear that the mean solar irradiance in the period between November and February is low compared to the remaining part over the year, and this will reflect on the temperature profile of the IBBC components. Furthermore, the average ambient temperature over the year is around 9.88 ^{o}C.

B. ISOLATED DC-DC BUCK-BOOST CONVERTER

The SRC-based IBBC has a high switching frequency input bridge (IB) in the front end, which is connected to a galvanic isolation transformer (TX). The resonant tank is coupled to the secondary winding of the transformer TX, and

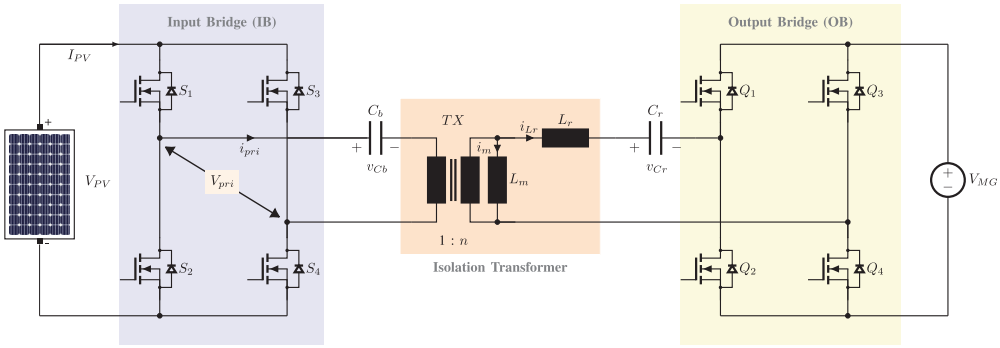


FIGURE 1. Configuration of the PV module-level system, where an SRC-based IBBC feeds MG.

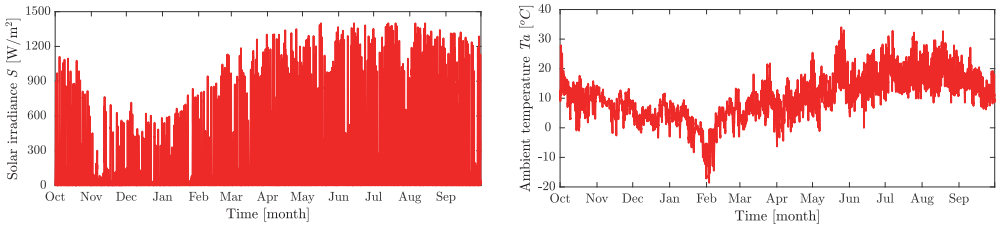


FIGURE 2. Yearly mission profile for Aalborg, Denmark: (a) solar irradiance and (b) ambient temperature.

the active output bridge (OB) is connected to the DC microgrid. The resonant tank compromises the resonant inductor L_r and the resonant capacitor C_r, and therefore the resonant frequency can be defined in (1). The blocking capacitor C_b before the transformer TX is employed to avoid the DC component in the transformer current, hence minimizing the conduction losses and avoiding the core saturation. It has a high capacitance value so that it has a negligible effect on the IBBC resonant frequency. Despite the studied IBBC based on the SRC has the same structure compared to the well-known LLC converetr, the employed SRC has a high ratio between the magnetizing inductance L_m and the resonant inductance L_r, and the resonant tank does not include L_m. On the other hand, the magnetizing inductance can be used as the resonant inductor in parallel with the resonant tank output port with the LLC converter. The literature regards this SRC design as series-resonant-converter operated in half-cycle discontinuous-conduction-mode [17], [18]. Therefore the given converter is regarded as SRC-based. The IBBC has both buck and boost functionality, despite the operation being at a fixed-switching frequency [15]. It employs varying the phase-shift between the right and left leg in the converter input bridge [13] in the buck mode for PV voltages above nominal (29 V in the given case) as shown in Fig. 3(a). At lower voltage, the secondary-side transistors needs to short-circuit the secondary winding to step-up the voltage [15] as shown in Fig. 3(b). Furthermore, the switching frequency should be lower than the resonant frequency by 5-10% [19]. The

TABLE 1 Parameters of the IBBC Converter

Parameter	Symbol	Value
Blocking capacitance	C_b	100 μF
Transformer turns ratio	n	12
Magnetizing inductance	L_m	2 mH
Resonant inductance	L_r	98.5 μH
Resonant capacitance	C_r	27 nF
Resonant frequency	F_r	97.5 kHz
Switching frequency	F_{sw}	95 kHz
DC MG voltage	V_{MG}	350 V

parameters of the studied IBBC are given in Table I, while the steady-state waveforms during the DCX mode are given in Fig. 4. The transformer turns ratio is selected to allow the converter produce the output voltage of 350 V at the nominal input voltage of 30 V typical for 60-cell Si PV modules. To design the resonant tank precisely, the relation between the resonance inductance L_r and the converter losses is shown in Fig. 5. It is clear that, with the large value of the resonant inductance, the losses of the converter can be reduced. However, the leakage inductance should be low enough to ensure resonant tank operation with discontinuous resonant current, i.e., Q factor less than one. The optimal value of the resonant inductance is approximately 100 μH. Next, C_r could be selected by knowing the required resonance frequency and the obtained value of L_r using (1). The magnetizing inductance must be calculated so that the magnetizing current can fully charge and discharge the parasitic output capacitance (C_{oss}) of the primary semiconductor during the dead time (T_{dt}) in the primary switches's gating signals as in (2). Additionally,

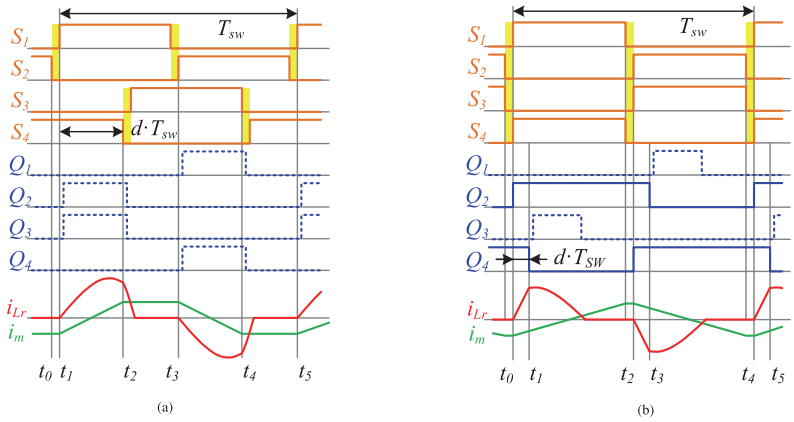


FIGURE 3. Modulation of the IBBC during the operation of (a) buck and (b) boost.

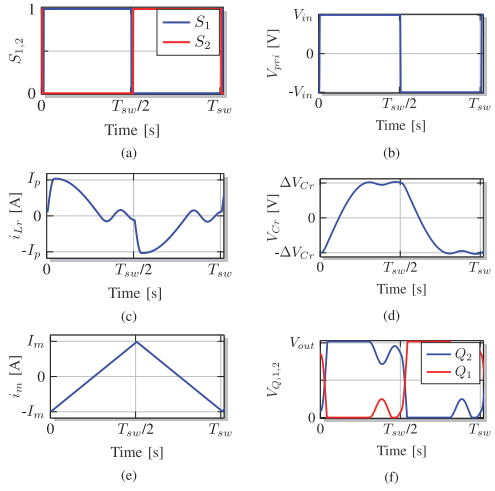


FIGURE 4. Ideal steady-state waveforms of the IBBC in the normal operation during one switching period: (a) Switching signal of $S_{1,2}$. (b) Primary winding voltage. (c) Resonant inductor current. (d) Resonant capacitor voltage. (e) Transformer magnetizing current. (f) Voltage across the OB switches $Q_{1,2}$.

Si FDMS86180 and SiC SCT2120AF MOSFETs are employed as the primary- and secondary-side semiconductors, respectively.

$$F_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

$$L_m \leq \frac{n^2 T_{dt}}{8 F_{sw} C_{oss}} \tag{2}$$

In the case-study IBBC, the IB is configured as a full-bridge, and its semiconductors in the same leg are operating in a complementary mode to avoid the short-circuit across the photovoltaic terminals. Moreover, a small dead-time is inserted between the gating signals of the IB semiconductors to allow the magnetizing current to discharge the parasitic output capacitance C_{oss} of the switches and therefore accomplish the zero voltage switching (ZVS) (thus, soft-switching feature) during the turn-on instant. The OB works as a full-bridge rectifier, and it could be turned off at zero current switching (ZCS) as the converter is designed to operate in the discontinuous conduction mode.

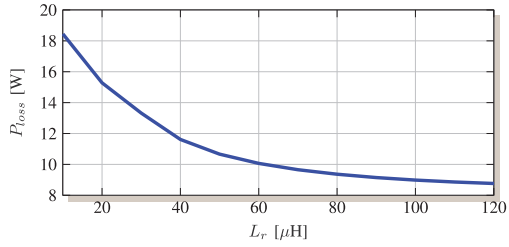


FIGURE 5. The dependence of the converter's total power loss on the resonant inductance value.

III. THERMAL MODELING OF THE IBBC COMPONENTS

Thermal modeling is a key stage in investigating the reliability of power electronic converters. The junction temperature of the MOSFETs (S_{1-4}, Q_{1-4}), as well as the hot spot temperature of the capacitors (C_b, C_r) and the isolation transformer (TX), can be obtained over the mission profile duration.

A. MOSFETs

Conduction losses in the IB and OB power devices depend on the RMS value of the switch current $I_{MOSFET,rms}$ and the on-state resistance, $R_{ds,on}$ as in (3). We consider the variation of $R_{ds,on}$ as a function of the junction temperature T_j [20] as well. The rise and fall times of the MOSFET lead to an overlap between the drain current and drain-source voltage of the switch so that some energy is lost during the switching instant. The methodology to calculate the MOSFET switching loss is adopted from the Infineon guidelines as in (4-5) [21]. However, the voltage rise and fall time is calculated using

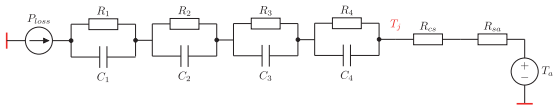


FIGURE 6. Thermal foster network of power semiconductors.

the accurate methodology by considering more points on the correlation curve between the switch voltage and the parasitic output capacitance as described in [22]. It is worth noting that for MOSFET switches, at turn-on, the body-diode continues to conduct during the current rise time. Turning off the body-diode of MOSFET requires removing any minority carriers stored in it, which must absorb reverse recovery energy, resulting in additional power dissipation. This dissipated power depends on the reverse-recovery charge (Q_{rr}) used in the power dissipation calculation, which can be taken from the MOSFET datasheet [21].

$$P_{MOSFET,cond} = R_{ds,on}(T_j)I^2_{MOSFET,rms} \tag{3}$$

$$P_{sw,on} = (V_{ds}I_{on}\frac{t_{ri}+t_{fu}}{2} + Q_{rr}V_{ds})F_{sw} \tag{4}$$

where V_{ds} is the drain-source voltage of the MOSFET during the turn-off state, I_{on} is the drain current at the beginning of turn-on instant, t_{ri} is the current rise-time, t_{fu} is the voltage fall-time, and Q_{rr} is the reverse-recovery charge.

$$P_{sw,off} = \left(V_{ds}I_{off}\frac{t_{fi}+t_{ru}}{2}\right)F_{sw} \tag{5}$$

where I_{off} is the drain current at the beginning of the turn-off instant, t_{fi} is the current fall time, and t_{ru} is the voltage rise-time.

Then, the MOSFET junction temperature can be estimated using the thermal impedance specified in the manufacturer datasheet using the foster model parameters as shown in Fig. 6, in which P_{loss} is the total losses of the semiconductors (i.e., P_{loss}=$P_{MOSFET,cond}$+$P_{sw,on}$+$P_{sw,off}$).

B. TRANSFORMER

It suffers from two types of losses, the conduction loss in the primary and secondary windings, and the second is the core loss. The conduction loss can be computed as

$$P_{Trans,cond} = R_{pri}I^2_{pri,rms} + R_{sec}I^2_{sec,rms} \tag{6}$$

where R_{pri} and R_{sec} are the ac resistance of the primary and secondary windings, respectively, while $I_{pri,rms}$ and $I_{sec,rms}$ are the RMS current of the primary and secondary windings, respectively.

As the flux in the transformer core of the IBBC is non-sinusoidal, e.g., it has a triangular shape when the voltage is applied to the primary winding, the improved general Stienmetz equation (iGSE) can be efficiently employed [23]. The magnitude of the flux density inside the core varies as a function of the voltage across the primary winding, which has a roughly square waveform in the considered case study. It is noteworthy that the isolation transformer is built using the RM14 core of 3C95 ferrite material using the Litz wire.

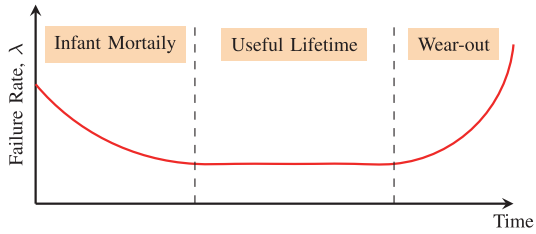


FIGURE 7. Bathtub curve of item hazard rate.

$$P_{Trans,core} = \frac{V_e k_i \Delta\beta^{\beta-\alpha}}{T_{sw}} \sum_m \left|\frac{B_{m+1}-B_m}{t_{m+1}-t_m}\right| (t_{m+1}-t_m) \tag{7}$$

where V_e is the effective volume of the transformer core, k_i, α, β are the Steinmentz coefficients that are obtained from the curve fitting in the core datasheet, B_m is the flux density in the core at the instant t_m, ΔB is the peak-to-peak flux density throughout the switching period. Then, the hot-spot temperature can be estimated using the thermal impedance (R_{th}) specified in the manufacturer datasheet as in (8), where P_{loss}=$P_{Trans,cond}$+$P_{Trans,core}$.

$$T_{hs} = T_a + R_{th}P_{loss} \tag{8}$$

C. CAPACITOR

The dielectric loss of the capacitor is ignored, and the power loss from the equivalent series resistance (ESR) is considered because of its significant effect by taking into account the dependency on the frequency as

$$P_C = ESR(f)I^2_{c,rms}(f) \tag{9}$$

where $I_{c,rms}$ is the RMS current of the capacitor.

Next, in a similar way to (8), the hotspot temperature of the capacitor can be computed using the capacitor thermal impedence and P_{loss}=P_C.

IV. RELIABILITY ANALYSIS

The hazard rate (i.e., failure rate) λ of the component denotes the conditional likelihood of the component to fail in a time interval, and it has the form of bathtub shape [24]. As shown in Fig. 7, the device has three regions of operation during its lifetime starting from the infant phase, where the hazard rate decreases over time, proceeding to the useful lifetime that has a constant hazard rate, and concluding by the wear-out phase, where the hazard rate starts to increase again. For many engineering applications, the power electronic converter is assumed to operate in the useful lifetime region, since it has a long life in practice [25].

A. APPROACH BASED ON MIL-HDBK-217F HANDBOOK

The MIL-HDBK-217F Handbook has been developed since the 1990 s by the United States Navy and is considered as an international standard for reliability prediction [26]. The models of the items inside it have been empirically verified.

TABLE 2 Parameters of IBBC Components With MIL-HDBK-217F Approach

Component	Parameter	Value
S_{1-4},Q_{1-4}	λ_b	0.012
	π_T	$\exp(-1925(1/(T_j+273)-1/293))$
	π_A	8
	π_Q	5.5
	π_E	1
C_b,C_r	λ_b	0.0005
	π_T	$\exp(2.5((T_a+273)/358)^{18})$
	π_V	$(Vs/0.4)^5$
	π_C	$1.6C^{0.13}$
	π_Q	30
	π_E	1
TX	λ_b	0.00159
	π_T	$\exp(((T_{hs}+273)/477)^{8.4})$
	π_Q	8
	π_E	1

The random failure rate of an item in the MIL-HDBK-217F reliability handbook has a multiplicative form where it is composed of multiplying the basic failure rate λ_b and π factors that indicate the stresses on the item such as (electrical, thermal, etc.) as in (10). The calculated random failure rate is expressed in the unit of failure/10^6 hours in the MIL-HDBK-217F.

$$\lambda = \lambda_b \left(\prod_{i=1}^{n} \pi_n \right) \tag{10}$$

where n is the number of π factors associated with the item depending on its category.

With the MIL-HDBK-217F handbook, the failure mechanism in MOSFET could be a defect in the substrate, solder connections due to the mismatch in thermal characteristics of MOSFET materials, and insulation films. It has four types of stress: temperature stress (π_T) that directly depends on the dissipated power in the device, application stress (π_A), quality factor π_Q, and environmental stress (π_E) that depends on the location of the item. Consequently, the failure rate of the MOSFET can be formulated as

$$\lambda_{\text{MOSFET}} = \lambda_b \pi_T \pi_A \pi_Q \pi_E. \tag{11}$$

The isolation transformer failure rate can be given as

$$\lambda_{\text{Trans}} = \lambda_b \pi_T \pi_Q \pi_E. \tag{12}$$

Finally, the capacitor failure rate can be expressed as

$$\lambda_{\text{Cap}} = \lambda_b \pi_T \pi_V \pi_C \pi_Q \pi_E \tag{13}$$

where π_C is the capacitance stress factor and π_V is the voltage stress factor.

The entire values for the factors of the IBBC components with MIL-HDBK-217F handbook are summarized in Table II.

B. APPROACH BASED ON FIDES GUIDE

The first version of the FIDES reliability handbook guideline was initialized in 2004 by eight French companies, and then it was upgraded in 2009 [27]. In this approach, the physics of failures is taken into account for predicting the random failure rate of the component, which is given by the unit of FIT (i.e., failure per 10^9 hours). The failure rate here is assumed constant during the lifetime, and the item does not enter into the wear-out phase during the mission profile period [28]. It is modeling the useful lifetime of the component, so it is not possible to evaluate the reliability of the component during the start-up stage [29]. Unlike the MIL-HDBK-217F reliability guidelines, the FIDES approach incorporates device technology, the influence of the extrinsic failure rate, and the sensitivity to quality factors from design to usage. It uses the annual mission profile for the item under study, and each mission profile can be divided into a set of phases, whose duration is defined in hours [30]. The FIDES guidelines are only relevant to ambient temperatures ranging from −55 °C to 125 °C, which is aligned with our mission profile. The general expression for an item failure rate can be given as

$$\lambda = \Pi_{\text{PM}} \Pi_{\text{Process}} \lambda_{\text{Phy}} \tag{14}$$

where Π_{PM} is the quality and technical control over manufacturing of the item, Π_{Process} comprises all the steps of item processes from specification to field operation and maintenance, and λ_{Phy} is the physical failure rate of the item, which can be calculated in the mission profile phase as

$$\lambda_{\text{Phy}} = \sum_{i}^{\text{Phases}} \left[\frac{t_{\text{annual}}}{8760} \right]_i \times (\lambda_i \Pi_i) \times (\Pi_{\text{Induced}})_i \tag{15}$$

where t_{annual} is the phase duration in hours during the year. The factor $(\Pi_{\text{Induced}})_{\text{i}}$ is the induced stress factor, which includes electrical, mechanical, or thermal stresses as

$$(\Pi_{\text{Induced}})_i = \left(\Pi_{\text{Placement}} \Pi_{\text{App}} \Pi_{\text{Rugg}} \right)^{0.511 \ln(C_{\text{sensitivity}})} \tag{16}$$

where $\Pi_{\text{Placement}}$ denotes the effect of the item placement in the system, Π_{App} represents the influence of the usage environment for application of the product contacting the item, Π_{Rugg} represents the influence of the policy for taking account of overstresses in the product development, and $C_{\text{sensitivity}}$ is the sensitivity of the item to over stress.

Consequently, the physical failure rate of the MOSFET device in the input and output bridges is described as

$$\lambda_{\text{Phy}-MOSFET} = \sum_{i=1}^{\text{Phase}} \left[\frac{t_{\text{annual}}}{8760} \right]_i \begin{pmatrix} \lambda_{0\,\text{TH}} \Pi_{\text{Thermal}} \\ +\lambda_{0TC\text{yCase}}\, \Pi_{TC\text{yCase}} \\ +\lambda_{0TC\text{ySolder joints}} \Pi_{TC\text{ySolder joints}} \\ +\lambda_{0\,\text{RH}} \Pi_{\text{RH}} \\ +\lambda_{0\,\text{Mech}} \Pi_{\text{Mech}} \end{pmatrix} \times (\Pi_{\text{Induced}})_i. \tag{17}$$

TABLE 3 Parameters of the IBBC Components With FIDES Approach

Component	Parameter	Value
Common Factors	Π_{PM}	1.42
	Π_{Process}	4
	$\Pi_{\text{Placement}}$	2.50
	Π_{APP}	3.20
	Π_{Rugg}	1.64
S_{1-4}	$\lambda_{0\text{TH}}$	0.0202
	$\lambda_{0TCy\text{Case}}$	0.00057
	$\lambda_{0TCy\text{Solder joints}}$	0.00285
	$\lambda_{0\text{RH}}$	0.0055
	$\lambda_{0\text{Mech}}$	0.000057
	$C_{\text{sensitvity}}$	5.60
C_b,C_r	$\lambda_{0\text{Cap}}$	0.05
	$\lambda_{\text{Thermal-electrical}}$	0.70
	λ_{0TCy}	0.28
	$\lambda_{0\text{Mech}}$	0.02
	$C_{\text{sensitvity}}$	6.05
TX	$\lambda_{0\text{Trans}}$	0.125
	$\lambda_{\text{Thermal-electrical}}$	0.01
	λ_{0TCy}	0.73
	$\lambda_{0\text{Mech}}$	0.26
	$C_{\text{sensitvity}}$	6.05
Q_{1-4}	$\lambda_{0\text{TH}}$	0.0202
	$\lambda_{0TCy\text{Case}}$	0.00303
	$\lambda_{0TCy\text{Solder joints}}$	0.01515
	$\lambda_{0\text{RH}}$	0.0589
	$\lambda_{0\text{Mech}}$	0.0003
	$C_{\text{sensitvity}}$	5.60

where

$$\begin{cases} \Pi_{\text{Thermal}} = e^{11604\times 0.7\times\left[\frac{1}{293}-\frac{1}{T_{mean}+273}\right]} \\ \Pi_{TCy\text{Case}} = \left(\frac{12\times N_{annual,cy}}{t_{annual}}\right)\times\left(\frac{\Delta T_{cycling}}{20}\right)^{4} \\ \times\, e^{1414\times\left[\frac{1}{313}-\frac{1}{T_{max,cycling}+273}\right]} \\ \Pi_{TCy\text{Solder joints}} = \left(\frac{12\times N_{annual,cy}}{t_{annual}}\right)\times\left(\frac{\min(\Theta_{cy},2)}{2}\right)^{\frac{1}{3}} \\ \times\, \left(\frac{\Delta T_{cycling}}{20}\right)^{1.9}\times e^{1414\times\left[\frac{1}{313}-\frac{1}{T_{max,cycling}+273}\right]} \\ \Pi_{\text{RH}} = \left(\frac{RH_{ambient}}{70}\right)^{4.4}\times e^{11604\times 0.9\times\left[\frac{1}{293}-\frac{1}{T_a+273}\right]} \\ \Pi_{\text{Mech}} = \left(\frac{G_{RMS}}{0.5}\right)^{1.5} \end{cases} \tag{18}$$

and the details and parameters definition can be found in [27]. The physical failure rate of the transformer equals in (19), while the capacitor physical failure rate is defined in (20). All values of the factors for the IBBC components are summarized in Table III for the FIDES approach.

$$\lambda_{\text{Phy-Trans}} = \lambda_{0\text{Trans}}\sum_{i=1}^{\text{Phase}}\left[\frac{t_{\text{annual}}}{8760}\right]_i \times \begin{pmatrix}\Pi_{\text{Thermo-electrical}} \\ +\Pi_{TCy} \\ +\Pi_{\text{Mechanical}}\end{pmatrix}_i \times (\Pi_{\text{Induced}})_i\,. \tag{19}$$

$$\lambda_{\text{Phy-Cap}} = \lambda_{0\text{ Cap}}\sum_{i=1}^{\text{Phase}}\left[\frac{t_{\text{annual}}}{8760}\right]_i \times \begin{pmatrix}\Pi_{\text{Thermo-electrical}} \\ +\Pi_{TCy} \\ +\Pi_{\text{Mechanical}}\end{pmatrix}_i \times (\Pi_{\text{Induced}})_i\,. \tag{20}$$

C. CONVERTER-LEVEL RELIABILITY PREDICTION

After specifying the random failure rate of each individual component (λ_n) in the IBBC, which is considered constant in the majority of the electronic components during their useful life, the component reliability over time (t) can be expressed as

$$R_n(t) = e^{-\lambda_n t}. \tag{21}$$

The mean time to failure (MTTF) refers to the time from the beginning until the first failure in the component occurs, and it is equal to the reciprocal of the failure rate, as in (22). In this study, the IBBC converter is expected to operate normally during the MTTF period and the converter is assumed to be a nonrepairable system with a minimal failure rate during the wear-out and infant mortality periods.

$$\text{MTTF} = 1/\lambda_n. \tag{22}$$

Once the failure rate of each component in the converter is determined, the overall failure of the IBBC converter can be recognized since it comprises eleven components (i.e., $N = 11$). In the current case study, the reliability block diagram is analyzed in a series connection, where if one component fails, the IBBC converter fails and malfunctions. Therefore, the IBBC failure rate can be given as

$$\lambda_{IBBC} = \sum_{n=1}^{N}\lambda_n. \tag{23}$$

Then, the reliability of the IBBC can be calculated by considering the product of the reliability of all system components as

$$R_{IBBC}(t) = \prod_{n=1}^{N}R_n(t) = e^{-\lambda_{IBBC}t}. \tag{24}$$

The overall flowchart for the reliability evaluation is given in Fig. 8. It starts with reading the PV mission profile of S and T_a, and then the thermal stress of the IBBC component could be defined using the look-up table synthesized based on the simulation of the IBBC. With the MIL-HDBK-217F reliability assessment approach, the thermal loading is directly considered without the need to use the rainflow counting algorithm that should be used in the FIDES approach. The input of the rainflow counting algorithm will be the component temperature (i.e., junction temperature of the MOSFETs, hotspot temperature of the capacitors and transformer). The results from the rainflow includes the peak-to-peak thermal cycle amplitude ($\Delta T_{cycling}$), cycle mean temperature (T_{mean}), and the cycle duration (Θ_{cy}). Then, this data helps to calculate the stresses across the component and thus the physical failure rate can be computed.

V. RESULTS AND DISCUSSION

The reliability assessment is implemented on GPU hardware using the Google Colaboratory notebook. A cloud software implementation of the FIDES approach for the IBBC was developed in Python to achieve high execution speed because its

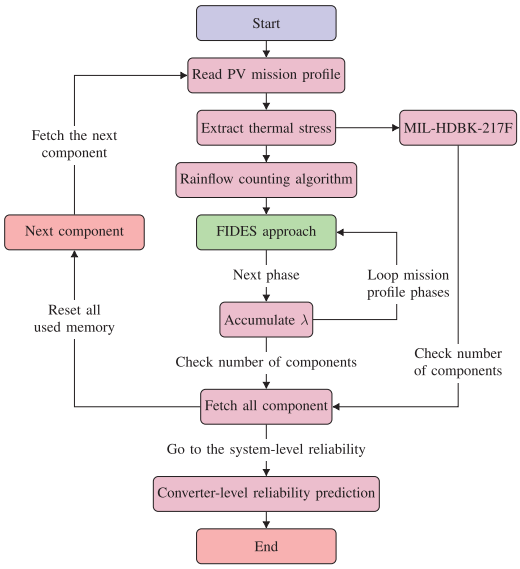


FIGURE 8. IBBC reliability prediction procedure from component-level to system-level.

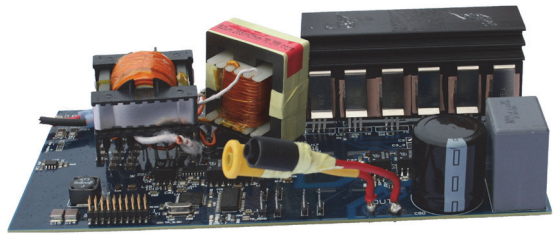
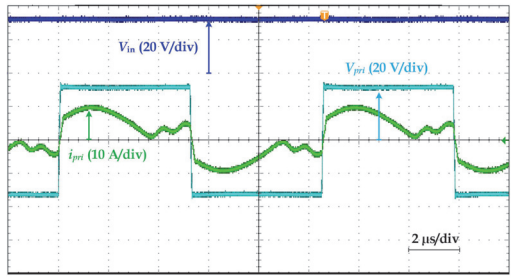
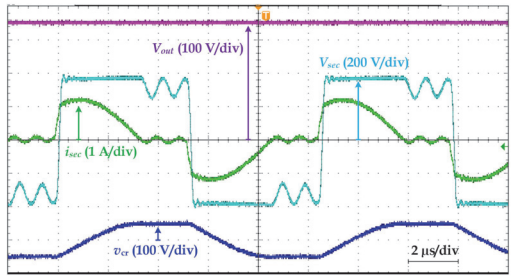


FIGURE 9. Experimental prototype of the studied converter.



(a)



(b)

FIGURE 10. Experimental waveforms for the steady-state operation of the IBBC at 200 W: (a) Primary side. (b) Secondary side.

implementation of scientific and numerical libraries is based primarily on optimized C code [31]. In this case study, the wear-out failure rate is ignored due to lack of 100/120 Hz ripples, and only the random failure rate over the useful lifetime is estimated [16]. The FIDES based approach considers the yearly mission profile of ambient temperature and solar irradiance, and thus the thermal stress over the year timespan is taken into account. From this point, the FIDES based approach can provide more accuracy to estimate the converter lifetime compared to the MIL-HDBK-217F based approach, which makes it suitable for reliability evaluation of the residential PV converters. The PV voltage at the maximum power is considered for evaluating the losses in the transformer TX core. The look-up table for thermal evaluation is created by modeling the system given in Fig. 1 using the PLECS software toolbox for MATLAB/Simulink environment. Additionally, the library of the rainflow counting algorithm is used to handle the non-uniform thermal profile of the IBBC component in order to evaluate its number of thermal cycles for using within FIDES reliability evaluation approach.

A. EXPERIMENTAL STEADY-STATE WAVEFORMS OF IBBC

The experimental setup is built in the laboratory as shown in Fig. 9. The built prototype is universal and allows for implementing different SRC topology configurations. The experimental waveforms of the converter in the steady-state operation are shown in Fig. 10. The operating power of the converter is 200 W. The converter is operating close to the DCX mode without any voltage bucking or boosting by controlling the duty-cycle, where the boosting action is resulted from the isolation transformer. The output voltage is fixed at 350 V for the DC microgrid applications. The secondary winding (resonant) current has a sinusoidal shape in both switching cycles. The primary current comprises of the secondary current and the magnetizing current as well.

B. THERMAL STRESS OF THE IBBC COMPONENTS

The temperature rise is considered the main source of the component failure, and it depends on the mission profile of the converter. Fig. 11 presents the PV power profile using the rainflow counting algorithm. The majority cycles of the PV power in the range between 50 W and 250 W, corresponding to the power cycle range less than 30 W. The power loss distribution in the IBBC at 180 W power is shown in Fig. 12. It is evident that the majority of the losses are dissipated in

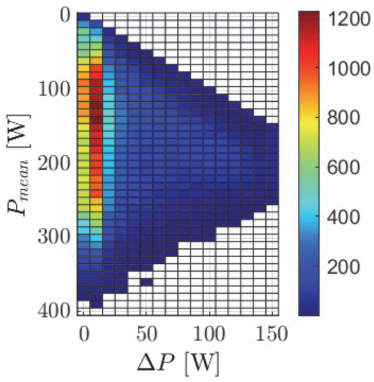


FIGURE 11. Rainflow analysis for the PV power cycle versus average power.

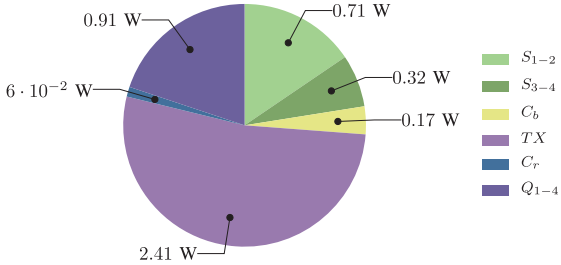


FIGURE 12. Distribution of the losses power of the IBBC at 180 W MPP of the PV module (i.e., total losses = $2S_{1-2}+2S_{3-4}+C_b+TX+C_r+4Q_{1-4}$ = 8.17 W).

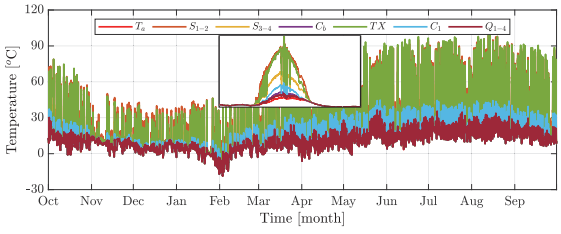


FIGURE 13. Annual thermal profile of the IBBC components.

the isolation transformer, while the resonant capacitor has the lowest value of losses.

The two semiconductors of the IB in the same leg share the thermal loading (due to the IBBC operation mostly in the buck mode during MPPT), while the whole OB semiconductors have the same thermal loading profile. Also, the switches, whose temperature profiles are equivalent, will have the same amplitude of thermal cycle, mean junction temperature, and maximum junction temperature as well. So the analysis from the rainflow counting algorithm will be identical for those components. Thus, the annual thermal profile of the IBBC components is shown in Fig. 13. The zoom view demonstrates

TABLE 4 Mean Temperature of Each IBBC Component Over the Yearly Mission Profile (I.e., Junction Temperature for Semiconductors and Hot Spot Temperature for Other Components)

Component	S_{1-2}	S_{3-4}	C_b	TX	C_r	Q_{1-4}
Temperature [°C]	17.70	13.64	10.46	16.06	10.94	10.25

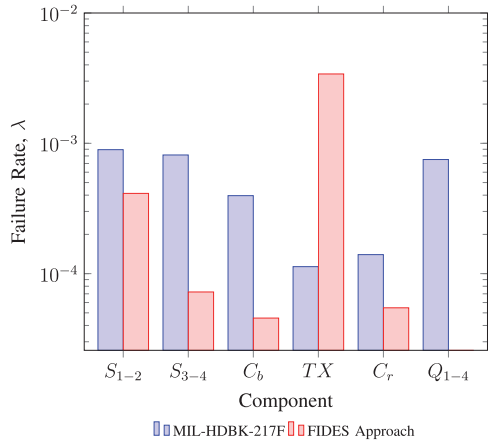


FIGURE 14. Annual failure rate of the IBBC component with the two reliability approaches.

that the primary semiconductors and the isolation transformer have the highest temperature profile. Furthermore, the mean temperature over the year is considered for the temperature stress factor in MIL-HDBK-217F calculations, as summarized in Table IV to overcome on independence on the mission profile.

C. FAILURE RATE PREDICTION

The failure rate of each IBBC component with the two reliability approaches is shown in Fig. 14. S_{1-2} features the highest failure rate among IBBC components with MIL-HDBK-217F approach, therefore it demonstrates the lowest reliability level. It is clear that the FIDES approach predicts a high transformer failure rate compared to the MIL-HDBK-217F approach, as it has a high basic failure rate of 0.125 FIT. By considering the total number of switches in IB and OB, the total failure rate (expressed in failure per year) of the IBBC with MIL-HDBK-217F and FIDES are 0.0071 and 0.0045, respectively (recalling (23)). The MTTF of the IBBC using the MIL-HDBK-217F and FIDES approaches is 141 and 219 year, respectively.

D. IBBC RELIABILITY PREDICTION

The IBBC reliability prediction is evaluated considering the random failure under the yearly mission profile for Aalborg, where the reliability of the converter due to aging with time is shown in Fig. 15. The converter begins with 100 percent reliability and then begins to deteriorate in an exponential fashion over time, where the B_{10} with MIL-HDBK-217F and

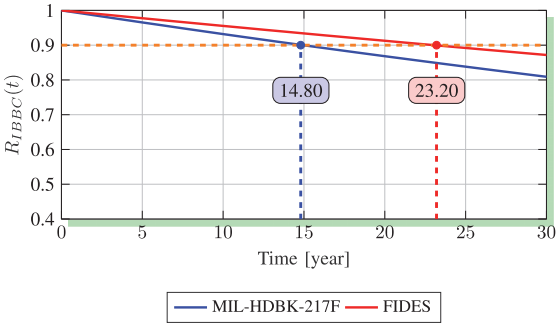


FIGURE 15. Reliability prediction of the IBBC converter over the time.

TABLE 5 Remarks on MIL-HDBK-217F and FIDES Based approaches [29]

MIL-HDBK-217F	• Internationally recognised and accepted handbook • Easy appropriation • Only one element in the mathematical formula • No explicit consideration for non-operating phases • Solder not integrated into component failure rate
FIDES	• Physics of failure • Consideration of the non-operating phases • External design and manufacturing defects are taken into account • A precise definition of the environment is required

FIDES have different values of 14.80 and 23.20 year, respectively. The key explanation for this disparity is that the two approaches have a different random failure rate for the IBBC (i.e., (24)). The results reported that the reliability of the PV system based on the IBBC at 25 years operation under Aalborg mission profile with MIL-HDBK-217F and FIDES is 83% and 89%, respectively. Consequently, the FIDES approach provides a reasonable prediction for the IBBC converter compared to the MIL-HDBK-217 approach. It is worth mentioning that the that analysis predicts mean values of random failure rates, while in practice, this process is stochastic.

E. COMPARISON OF MIL-HDBK-217F AND FIDES BASED APPROACHES

The MIL-HDBK-217F handbook can be used with different applications like military aeronautics, military automobile, and military ground installation. However, it is unsuitable for civil use and provides pessimistic reliability predictions in civil applications. While FIDES guide based approach can be integrated in civil aeronautics, aircrafts, and naval military equipment. In addition, it provides a realistic reliability predictions when developing electronic products, and provides engineering processes and tools to evaluate the reliability of systems. It includes the component technology, type of application, life cycle, overstresses, and actual conditions during the usage, to evaluate the component reliability. Furthermore, FIDES guide takes into account the extrinsic failure rate. The main remarks of both reliability guidelines are given in Table V.

VI. CONCLUSIONS AND FUTURE WORK

The paper has discussed the reliability of IBBC based on the SRC for PV applications under a yearly mission profile using two reliability assessment approaches. To obtain the thermal stress, the losses of the IBBC component have been carefully modeled. The results show that FIDES guide approach takes into account the real mission profile obtained in the field. The approach based on the MIL-HDBK-217F handbook ignores the mission profile, which becomes out of date. Therefore, FIDES guide is considered to provide a more realistic lifetime prediction based on well-established empiric models for the PV converter based on the IBBC. On the other hand, MTTF is an average value that describes a stochastic process that should follow some probability distribution, when some converter will fail before reaching that time and some after it. The obtained results prove the main assumption that the primary side semiconductors significantly contribute to the system random failure rate, while the influence of the output-side switches can be neglected. In addition, the FIDES approach introduces high basic failure rate for the transformers, which makes the transformer the least reliable passive component in the IBBC for PV applications.

The future work of the paper will focus on demonstrating the reliability of the IBBC at different operating modes. Also, the effect of the double line frequency would be considered in case of being connected to a single-phase AC grid via a back-end inverter.

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Self-Healing Photovoltaic Microconverter with Zero Redundancy and Accurate Low-Cost Fault Detection

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***Abstract*—This paper studies a zero-redundancy fault-tolerant dc-dc series resonant converter (ZR-SRC) for residential photovoltaic (PV) applications. This converter can handle faulty conditions on-the-fly using topology morphing control without increasing the number of components. Furthermore, it can withstand a single fault in both input and output bridge semiconductors, i. e., up to two semiconductor faults. The proposed dc-dc converter could increase the availability of residential photovoltaic-powered dc microgrids. Comprehensive fault diagnosis and localization algorithms are proposed for MOSFETs on both sides of the ZR-SRC. The paper proposes a short-circuit fault (SCF) detection in the input-side MOSFETs using the existing PV voltage measurements, decreasing the converter cost and size. The open-circuit fault (OCF) in the output-side MOSFETs is detected by sensing the voltage of the bottom two switches sharing the same ground with the dc bus. In addition, the post-fault operation of the converter is thoroughly analyzed. Recommendations for the PV power clipping are given to ensure the safe operation of the converter after a fault. A 300 W experimental setup is built to demonstrate the feasibility and performance of the proposed fault-tolerant converter.**

***Index Terms*—Fault tolerance, dc-dc converters, Photovoltaics, Reliability, Fault diagnosis, Fault detection.**

NOMENCLATURE

ZR	Zero redundancy
SRC	Series resonant converter
PV	Photovoltaic
MOSFET	Metal-oxide-semiconductor field-effect transistor
SCF	Short-circuit fault
OCF	Open-circuit fault
FT	Fault-tolerant
IGBT	Insulated-gate bipolar transistor
DAB	Dual active bridge
qZS	Quasi Z-source
IB	Input bridge
OB	Output bridge
TMC	Topology morphing control
PSM	Phase shifted modulation
APWM	Asymmetrical PWM
FHR	Forced half-resonance
FB	Full-bridge
HB	Half-bridge
MG	Microgrid
LLC	Inductor-inductor-capacitor
MPPT	Maximum power point tracking
Bk	Buck mode
Bt	Boost mode

I. INTRODUCTION

DIRECT current (dc) microgrids provide high efficiency and allow for direct connection of energy sources, energy storage, and dc loads. This creates an emerging market for dc-dc converters that satisfy requirements of high power density, high efficiency, wide input voltage regulation, and high reliability. During the power converter selection among the products available on the global market, its reliability has a high priority level for mission-critical applications such as medical devices, aircraft, data centers, etc. [1]. By increasing reliability, the converter improves its availability during long-term operation. According to industrial statistics, power semiconductors represent around 40% of power electronic converter failures [2]. One of the possible ways to increase the reliability of power electronics converters is to apply fault-tolerant (FT) techniques. An FT converter can provide continuity for various services in the case of a component fault.

The semiconductors faults could be broken into open-circuit faults (OCFs) or short-circuit faults (SCFs). The drift of the parameters could lead to high power losses in the device and, therefore, a high junction temperature, which could result in a switch failure in OCF or SCF [3]. The SCF could cause excessive stress on the components if not remedied. Quick detection and precise localization of a fault require a proper fault diagnosis technique. Fault identification is used to locate the failed component in the system. There are signal-based and model-based fault detection methods for dc-dc converters [4].

With the model-based methods, the actual values of the converter diagnosis signals are measured and then compared with estimated values. The well-known approaches for estimation are the Kalman filter [5], extended Kalman filter [6], slide mode observer [7], and Luenberger observer [8]. Based on the deviation between the measured and estimated values, the converter state (i.e., healthy or faulty state) can be identified.

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The signal-based methods perform time-domain or frequency-domain analysis of the diagnosis signal. The time-domain methods use a simple and low-cost analog implementation to compare the diagnosis signals with a threshold level [9]. The frequency-domain methods employ Fourier Fast Transform to extract the information about the converter status [10]-[11]. The frequency-domain analysis has the drawback of high computational effort and complexity.

Several approaches can be utilized to improve power converter reliability. The simplest way is to overdesign the converter to achieve higher reliability at the expense of the associated cost. The conventional solutions based on (N + 1) redundancy suffer from a high realization cost rendering it unpractical in many applications [12]. Component-level redundancy could be implemented by adding an extra active leg to a dc-dc converter, like in the series resonant converter (SRC) presented in [13]. Although its components will not be overstressed after a fault, the cost of the extra bridge leg and its gate-driving circuitry is high. In addition, a fuse is needed to isolate the SCF. It can handle both OCF and SCF but is limited to IGBT switches as they can withstand high currents long enough for a fuse to burn. In [14]-[15], the capacitor leg is used to reconfigure the SRC into a voltage doubler on the output side.

In some examples of FT isolated dc-dc converters, fault tolerance is not fully implemented but requires additional components. An FT dual active bridge (DAB) converter proposed in [16] requires a high number of components but withstands only OCFs in IGBTs by reconfiguring the central-tapped transformer. The topology morphing control introduced in [17] for a qZS PV microconverter shows how to simplify the design of FT dc-dc converters. Fault detection could also be simplified by reusing existing components, like detecting the inductor voltage signature via an extra winding [18].

A few research articles have addressed the fault tolerance of the SRC, despite its advantages. The fault diagnosis in the isolated step-up SRCs was not well analyzed. Several attempts have been made to diagnose a single fault type. This paper studies zero-redundancy SRC (ZR-SRC) that can provide FT operation without extra components. It can withstand up to two faults before malfunctioning. Based on previously evaluated failure rates, this study addresses both SCF and OCF. The first version of the studied converter was introduced in [19]. The contributions of this paper could be summarized as follows:

1. Development of a buck-boost FT converter based on SRC with zero redundancy and post-fault power clipping control allowing to avoid of efficiency drop and new faults.
2. A new low-cost and accurate diagnosis technique to detect the SCF in the input-side MOSFETs exploiting the existing voltage measurements at the input PV terminals.
3. A new low-cost and accurate OCF/SCF diagnosis and detection methodology for the output-side MOSFETs.
4. Converter post-fault on-the-fly reconfiguration algorithm.
5. First demonstration of an isolated FT dc-dc converter operational after two subsequent semiconductor faults.
6. PV power clipping algorithm that maintains the failure rate of the ZR-SRC components unchanged during the post-fault operation, with a minimum reduction of energy harvest.
7. Experimental verification of the proposed fault diagnosis and tolerance using a laboratory prototype rated at 300 W.

Below, Section II describes the ZR-SRC operation in normal conditions and its design guidelines. Then, the proposed fault diagnosis and localization in the input bridge (IB) and output bridge (OB) are discussed in Section III. The post-fault operation of the converter is analyzed in Section IV. The experimental validation of various scenarios is presented in Section V, and finally, the conclusions are drawn in Section VI.

II. Zero-Redundancy Fault-Tolerant SRC

The complete structure of the ZR-SRC topology is given in Fig. 1. The basic concept of ZR-SRC is based on the topology morphing control (TMC) that allows the converter to continue its operation after a fault without adding more components. It has been demonstrated for the first time in [19]. Generally, it has two hybrid switching cells, one on the input side (IB) and the other on the output side (OB).

In this paper, the ZR-SRC is used for interfacing a residential PV module into a dc microgrid with a stiff voltage V_{MG} and high capacitance. Thus, after an OCF occurs in the OB bottom MOSFETs (Q_2 or Q_4), the converter operation will be restored using the OB top MOSFETs (Q_1 and Q_3) – one of them should be turned on or off in case of OCF or SCF, respectively. The top MOSFETs are used instead of diodes to enable fault-tolerant operation. Their body diodes are employed as rectifier diodes during normal operation, keeping the number of discrete semiconductors unchanged. The synchronous rectification is not used to prolong the lifetime of MOSFETs by constraining the degradation of their gate oxide layers [20]. These two measures result in a slight reduction in efficiency.

A. Converter Operation

In Fig. 1, MOSFET devices include parasitic elements. The resonant inductor L_r could be integrated into the high-frequency transformer to improve power density [5]. The switching frequency f_{sw} should be selected at less than 5-10% of the resonant frequency f_r as given in (1), in which C_r is the resonant capacitance [21]-[22]. The blocking capacitor C_b removes any dc bias current in the transformer while enabling switching cell reconfiguration. It has a negligible effect on the resonant frequency if $C_b \gg C_r \cdot n^2$, where n is the transformer turns ratio.

The ZR-SRC can buck or boost the input voltage at a fixed switching frequency, which leads to the capability of regulating wide input voltage variation. There are different PWM techniques for the ZR-SRC operating at a fixed switching frequency, such as phase shifted modulation (PSM) [23], asymmetrical PWM (APWM) [24], interleaved PWM [25], and forced half-resonance (FHR) PWM [26].

The steady-state waveforms of the ZR-SRC using these PWM techniques are depicted in Fig. 2, considering the normal and post-fault operation for the faults shown in Fig. 2c. The PSM and APWM techniques are employed for buck operation when the PV voltage exceeds the nominal value by adjusting the phase shift between the two legs of the front-end inverter. The PSM in Fig. 2a is applied in the case of the full-bridge (FB) operation of the front-end inverter, while the APWM in Fig. 2d is employed in the case of its half-bridge (HB) post-fault operation. With the PSM, the conduction losses in the body

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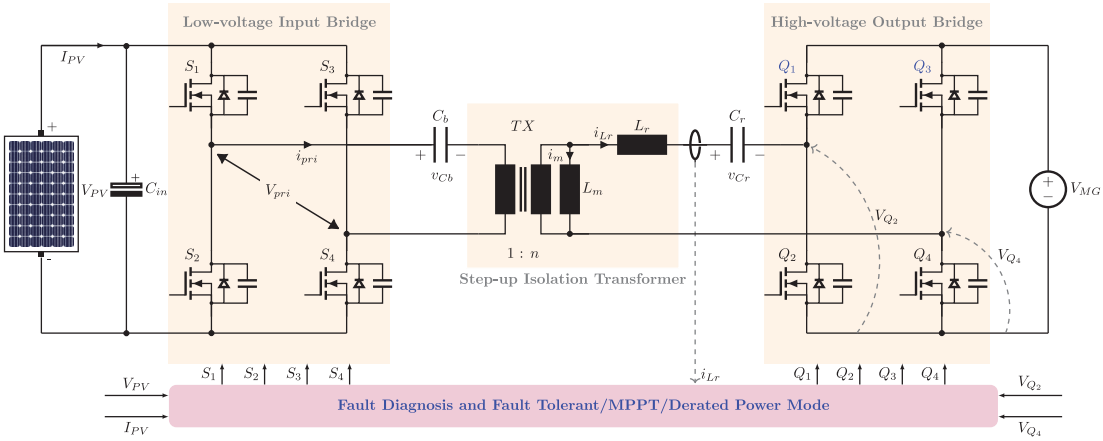
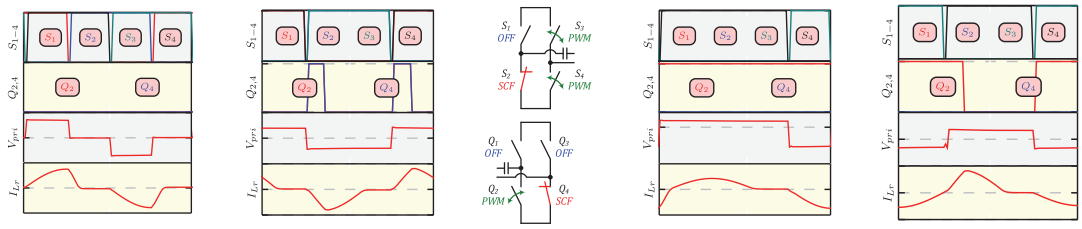


Fig. 1. The ZR-SRC topology for residential PV integration into dc MG, including the measurement signals for MPPT and fault diagnosis.



(a) (b) (c) (d) (e)

Fig. 2. Steady-state waveforms of ZR-SRC for one switching period using different PWM methods: a) FB-FB with normal buck operation (PSM), b) FB-FB with normal boost operation (interleaved PWM), c) considered examples of semiconductor faults, d) HB-HB with post-fault buck operation (APWM), and e) HB-HB with post-fault boost operation (FHR).

diodes of the IB MOSFETs are eliminated [27]. In contrast, the APWM provides a long conduction interval, which makes the resonant current half-wave sinusoidal. This leads to improving the soft-switching of the converter and, thus, better efficiency. At the same time, the secondary-side transistors need to short-circuit the secondary winding to step up the voltage when the PV voltage is below the nominal value using interleaved and forced half-resonance PWM techniques, i.e., modulation from Fig. 2b, is employed for full-bridge rectifier operation. The modulation in Fig. 2e applies to the voltage doubler (half-bridge) rectifier. In these two cases, the resonant inductor is first charged with energy from the input side. It releases this stored energy to the load. In Fig. 2e, the resonant inductor features FHR with a half-cycle sinusoidal shape, which improves converter efficiency by eliminating one hard turn-on of the OB MOSFETs.

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}} \tag{1}$$

B. Design Guidelines

Firstly, the transformer turns ratio (i.e., n) is chosen so that the ZR-SRC can generate the output voltage of 350 V, i.e., the most common dc MG voltage, at the nominal input voltage of 30 V ($V_{\mathrm{IN,nom}}$) typical for 60-cell Si PV modules as in (2).

$$n = \frac{V_{MG}}{2V_{IN,nom}} \tag{2}$$

The number of turns in the primary winding must be optimized to avoid saturation. On the other hand, the leakage inductance has to be high enough to improve the converter efficiency, as shown in [27], but low enough to ensure ZR-SRC operation in the discontinuous resonant current mode:

$$L_r < \frac{2 \cdot n^2 \cdot V_{IN,\min} \cdot f_{sw}}{I_{IN,\max} \cdot \omega_r^2}, \tag{3}$$

which depends on the minimum input voltage $V_{IN,min,}$ and maximum input current $I_{IN,\ max}$. It could be recommended to select L_r in the range of 60..70% of the critical value in (3) to account for losses and non-modeled dynamics in the converter.

The magnetization inductance L_{m} should be able to fully recharge the parasitic output capacitances (C_{oss}) of the primary semiconductor during the dead time (T_{DT}), as

$$L_m \le \frac{n^2 \cdot T_{DT}}{8 \cdot f_{sw} \cdot \mathrm{C_{oss}}}. \tag{4}$$

Knowing the values of L_r and f_r, the resonant capacitor C_r can be directly defined using (1). It is worth mentioning that the average voltage of the resonant capacitor equals zero in the normal full-bridge rectifier operation and has a considerable dc bias in its post-fault half-bridge operation. The peak-to-peak

voltage ripple across C_r (ΔV_{Cr}) is affected by the converter output power P_{out} and the PV module voltage, as

$$\Delta V_{Cr} = \frac{P_{out}}{2 \cdot n \cdot V_{PV} \cdot f_{sw} \cdot C_r}. \quad (5)$$

The voltage stress of semiconductor components equals the maximum operating voltage of the corresponding port. The proposed concept avoids overrating the components. Hence, they should be designed for the current stress in normal operation. Explicit expressions for the switch current stress are provided in [22]. This converter utilizes non-overlapping modulation of the output switches in normal operation in the full-bridge boost mode, which offers better stability at the cost of lower efficiency [21]. Its reliability analysis for PV applications was previously published in [28].

III. Proposed Fault Diagnosis and Detection Routine for ZR-SRC Based Residential PV

This study considers both OCF and SCF of semiconductors. The best practice is to utilize Si MOSFETs in the IB and SiC in the OB. Generally, SRC and LLC topologies are widely adopted in many industrial applications, such as data centers and battery chargers, due to their soft switching and high-efficiency features [21]. A recent survey covering a wide range of practicing engineers and academic researchers from different countries was conducted about the failure of these converters [29]. About 72% of the participating companies have more than ten years of market experience. The summary of this detailed survey indicates that the primary semiconductors of the SRC/LLC converters are regarded as the main source of converter failure. It contributes approximately half of the damage source of the converter. Also, respondents reported that primary semiconductors typically show SCFs. Furthermore, we have collected random samples of failed low-voltage switches that have been tested in the laboratory for high step-up dc-dc converters for a long time [30]. The quantitative results prove that the SCF fits 100% of the collected dataset. The resulting statistical analysis of the collected dataset is consistent with the results collected for the SRCs in industrial applications [29]. In line with the previous discussion, the study of this paper will consider only the SCF of the primary semiconductors during fault diagnosis and detection. Additionally, a study [30] reports 18/82% distribution for OCF/SCF of high-voltage SiC MOSFETs in the OB of the ZR-SRC topology, which necessitates their detection and identification in this converter.

The fault must first be detected using an appropriate signature signal that adequately describes the converter operation in every state. To truly decide whether to reconfigure the converter after the signature signal triggers the failure mode, the fault location may need to be defined. The fault detection routine monitors continuously the converter state and provides rapid identification and on-the-fly reconfiguration, which is an advantage compared to the closest competing solution [17].

A. Input-Side SCF Diagnosis and Localization

The studied ZR-SRC is aimed at residential PV applications. It ensures PV module operation at the maximum power point using a maximum power point tracking algorithm. This converter is capable also of performing the global MPPT. The PV module voltage and current are both necessary measurements for the MPPT (i.e., V_{PV} and I_{PV}, respectively). By its very nature, the PV module is a limited current source, with a short-circuit current that is not excessively high compared to that at the maximum power point (MPP), in which the converter operates before a fault. Thus, an SCF in one of the IB MOSFETs could not harm the converter components if detected fast enough.

Most literature focuses on studying the faulty state of the power electronic converter while treating the input source as a rigid voltage power supply (even if the input source is PV), which implies that the current will be high and increase rapidly after the fault existence. This work proposes using the existing input voltage measurement to diagnose SCFs in IB MOSFETs to avoid the additional cost and size of including additional sensing components, which distinguishes this method from the existing solutions. When one of the IB switches experiences SCF, the PV voltage begins to fall from the V_{MPP} to zero at a rate influenced by the input capacitance of the PV module and the drain-source resistances of the defective and healthy switches in the same leg. The healthy switch is turned on under the specific modulation signal in this particular instance. Therefore, the significant variation in the PV voltage indicates that the IB switches are malfunctioning.

Once the diagnosis condition has triggered the SCF fault, its precise location in the left or right leg should be determined. As the defective leg becomes inactive due to disabled gating signals, it is not always possible to identify precisely which MOSFET in the IB is defective. It is worth noting that the proposed algorithm does not need to identify the fault location accurately. Instead, only the faulty leg needs to be identified, i.e., the left or right leg. If we assume that the left leg is faulty, both gate signals of leg switches (S_1 and S_2) should be disabled. After a brief time, milliseconds, the PV voltage should be measured to verify that it is restored.

In this manner, it is unnecessary to check the sign of the primary winding voltage or incorporate test switching patterns into the detection routine, like in [17]. The design of the detection routine is subsequently made simpler and more feasible. The process of diagnosis and detection of SCF in IB MOSFETs is described in Algorithm 1.

Algorithm 1. SCF diagnosis and detection routine for IB MOSFETs

```
At first, the ZR-SRC is operating at MPPT.
Measure the PV voltage (V_PV) and current (I_PV)
If (V_PV == 0) then
    Trigger SCF in IB MOSFETs
    Apply the PWM pattern by assuming that the left leg is faulty
    Wait for 3-time units of the ADC trigger timer until the input capacitor recharge
        If (V_PV > 0) then
            SCF in the Left leg
        else
            SCF in the right leg
        End if
End if
```

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B. Output-Side OCF Diagnosis and Localization

To identify the OCF in the OB MOSFETs, the voltage of the bottom switches is sensed, as shown in Fig. 3. The main reason for choosing voltages of the bottom switches is that they share a common ground, which minimizes the number of isolated power supplies for the sensors. Due to the parasitic capacitances of the converter semiconductors, the resonant current oscillates around the zero axis when the OCF occurs in the output-side full-bridge MOSFETs, interrupting the operation of the converter. The body diode of the malfunctioning switch becomes inactive with the OCF and cannot clamp negative voltage oscillations. Therefore, the voltage swing on the faulty switch increases, resulting in an easily recognizable voltage step at the output of the sensing circuit from Fig. 3. The OCF state in the OB has no impact on the input-side waveforms of the primary voltage or the magnetizing current. A decision must be made after the OCF detection to reconfigure the converter appropriately. Each bottom switch in the output-side rectifier has its detection and localization circuit. As a result, the OCF in the OB can be triggered and identified at the same instant. The expression of the rectified voltage of the bottom diodes (V_{rec}) during the pre-and post-fault operation (i.e., OCF at the OB MOSFETs) when the converter is operated at the rated power, can be given as:

$$V_{rec} = \begin{cases} 2V_{MG} & Pre-fault\ operation \\ 4V_{MG} & Post-fault\ operation \end{cases} \quad (6)$$

where V_{MG} is the DC microgrid voltage that is assumed to be constant in the current study.

C. Output-Side SCF Diagnosis and Localization

The signature signal for triggering the SCF in the OB rectifier is the resonant inductor current I_{Lr}, which begins to increase when the SCF occurs in one of the OB bottom switches. Due to the low secondary current in the step-up transformer, a low-cost current transformer is needed to sense I_{Lr}. The sensed inductor current is a bipolar signal, so it is best to rectify it using the low-power full-bridge rectifier. The rectified signal is filtered and measured by a comparator embedded in the microcontroller. The flowchart of the proposed SCF detection algorithm is shown in Fig. 4. The interrupt routine of the comparator of the microcontroller will be run to change the modulation scheme and protect the transformer windings from the high current once the secondary current reaches the predetermined threshold level. The threshold level of the secondary winding current I_{th} can be adjusted according to the operating power. However, the threshold value should be defined with some tolerance to allow for regulation transients.

IV. Post-Fault Operation of the ZR-SRC

Once the converter enters the faulty state, it should be recovered using TMC to continue MPPT from the photovoltaic module under current environmental conditions. The possible PWM switching patterns for both IB and OB are summarized in Table I. The corresponding state transitions are visualized in Fig. 5. These switching patterns result from the assumption that IB and OB operate simultaneously as FB or HB, depending on the state of the ZR-SRC, either healthy or faulty. The FB operation is used in the normal state (no faults in IB/OB), while the HB operation is considered in the faulty state. In both configurations, the ZR-SRC can buck or boost the input voltage. The IB MOSFETs perform voltage bucking, whereas the OB MOSFETs perform voltage boosting.

The efficiency of the FT dc-dc converters typically degrades after a fault, and the efficiency drop can vary significantly depending on the mode of operation of the converter [17]. This observation raises an issue related to the overloading of the main components when attempting to operate near the rated power after the topology reconfiguration due to the fault. If a zero-redundancy FT converter continues to deliver rated power after the fault, the lifetime of healthy components could be shortened as they are subjected to high thermal stress or even catastrophic failure. The likeliness of this case depends on design tradeoffs. For example, low-cost designs use smaller PCBs and cheaper semiconductors to meet cost targets and cannot provide sufficient cooling to operate at a rated power after a fault. As a result, low-cost implementations of zero-redundancy FT dc-dc converters may require introducing a

TABLE I.
POSSIBLE SWITCHING PATTERNS OF ZR-SRC FOR IB AND OB AT DIFFERENT FAULT STATUS

Primary Side										Secondary Side									
P	S_1	S_2	S_3	S_4	Mode	PWM	Duty-cycle	Status	Type	S	Q_1	Q_2	Q_3	Q_4	Mode	PWM	Duty-cycle	Status	Type
0	PWM	PWM	PWM	PWM	Buck	PSM	MPPT	Normal	FB	0	OFF	OFF	OFF	OFF	-	-	0	Normal	FB
1	OFF	ON	PWM	PWM	Buck	APWM	MPPT	Normal	HB	1	OFF	ON	OFF	OFF	-	-	0	Normal	HB
2	SCF	OFF	PWM	PWM	Buck	APWM	MPPT	Faulty	HB	2	ON	OCF	OFF	OFF	-	-	0	Faulty	HB
3	OFF	SCF	PWM	PWM	Buck	APWM	MPPT	Faulty	HB	3	OFF	OFF	ON	OCF	-	-	0	Faulty	HB
4	PWM	PWM	SCF	OFF	Buck	APWM	MPPT	Faulty	HB	4	OFF	SCF	OFF	OFF	-	-	0	Faulty	HB
5	PWM	PWM	OFF	SCF	Buck	APWM	MPPT	Faulty	HB	5	OFF	OFF	OFF	SCF	-	-	0	Faulty	HB
6	PWM	PWM	PWM	PWM	-	-	0.5	Normal	FB	6	OFF	PWM	OFF	PWM	Boost	Interleaved	MPPT	Normal	FB
7	OFF	ON	PWM	PWM	-	-	0.5	Normal	HB	7	OFF	ON	OFF	PWM	Boost	FHR	MPPT	Normal	HB
8	SCF	OFF	PWM	PWM	-	-	0.5	Faulty	HB	8	ON	OCF	OFF	PWM	Boost	FHR	MPPT	Faulty	HB
9	OFF	SCF	PWM	PWM	-	-	0.5	Faulty	HB	9	OFF	PWM	ON	OCF	Boost	FHR	MPPT	Faulty	HB
10	PWM	PWM	SCF	OFF	-	-	0.5	Faulty	HB	10	OFF	SCF	OFF	PWM	Boost	FHR	MPPT	Faulty	HB
11	PWM	PWM	OFF	SCF	-	-	0.5	Faulty	HB	11	OFF	PWM	OFF	SCF	Boost	FHR	MPPT	Faulty	HB

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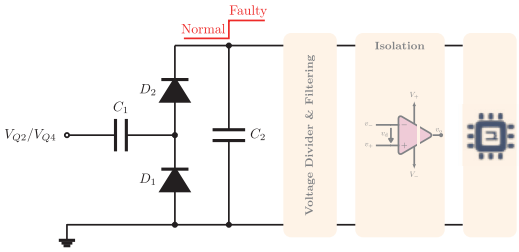


Fig. 3. The voltage sensing circuit for each of the bottom OB switches to diagnose and detect the OCF in the output-side MOSFETs.

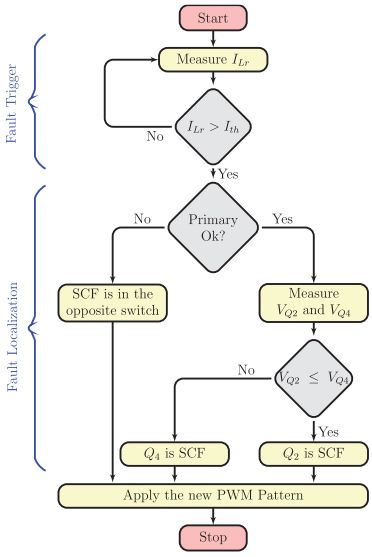
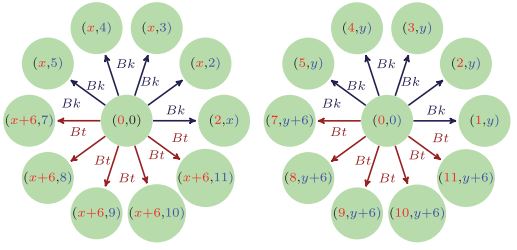


Fig. 4. Flowchart to diagnose and identify the SCF in the OB MOSFETs.



(a) (b)

Fig. 5. ZR-SRC state machine transition (red refers to P and blue refers to S in Table I, *Bk* refers to the bucking mode and *Bt* refers to the boosting mode) for a) IB MOSFETs ($x \in \{2,3,4,5\}$ for SCF in $\{S_1, S_2, S_3, S_4\}$, respectively) and b) OB MOSFETs ($y \in \{2,3\}$ for OCF in $\{Q_2, Q_4\}$ and $y \in \{4,5\}$ for SCF in $\{Q_2, Q_4\}$, respectively).

software constraint (clipping) of input power into the control system to ensure the safe operation of the converter after a fault. However, in many applications, including photovoltaics, operation at maximum power occurs infrequently and accounts for only a tiny portion of the yearly energy output.

The energy generation of the photovoltaic system should be weighed against the reliability of the converter. Operation below maximum output allows for avoiding overloading healthy components of a faulty converter, i.e., avoiding catastrophic failure [28]. This way denotes the power clipping mode for PV operation. Any power other than the maximum power can be achieved at two values of PV voltage; in other words, the PV voltage is to the left or the right of the MPP voltage. In practice, reducing power above the MPP voltage is more advantageous because high step-up converters typically offer higher efficiency at lower dc gain [32]. Algorithm 2 describes the photovoltaic power clipping strategy that prevents the ZR-SRC from becoming overloaded after a fault. Before starting the converter, the open-circuit voltage of the PV terminal is recorded at $I_{PV} = 0$. Then, at each cycle of the MPPT algorithm execution, the recorded power value is compared to the actual PV power, defining ΔP. The converter should operate on the left-hand side of the P-V curve to limit input voltage variations and, thus, achieve higher efficiency. Therefore, the PV voltage should not be lower than 75% of the recorded open-circuit voltage that does not change too much with the irradiation. Then, the input power is kept under the predefined level by adjusting the converter duty cycle when the clipping power mode is activated. In case of the maximum PV power is lower than the power curtailment level, the conventional P&O algorithm defines the duty cycle to track the PV module MPP at the current weather conditions. In that case, the converter could not be overheated during the post-fault operation.

Algorithm 2. Photovoltaic power clipping method

```
Read the open-circuit voltage (V_OC) at I_PV = 0 at starting the ZR-SRC
Set ΔP = P_max_level - V_PV × I_PV
If (V_PV < 0.75 × V_OC) then
    Set d= d + Δd
    Else If (ΔP < 0) then
            Set d= d + Δd
        else
            Calculate d based on MPPT
        End If
End If
```

V. Experimental Results and Discussion

A 300 W prototype was built in the laboratory, as shown in Fig. 6. Its parameters and components are listed in Table II. The resonant inductor was embedded into the transformer with a hybrid split bobbin design. The digital platform here is the STM32F334 microcontroller, which offers high performance at a low cost. The experimental setup for data logging is shown in Fig. 7. It employs a solar array simulator Agilent E4360A to emulate the 60-cell Si PV module and record the instantaneous PV voltage and current, as well as PV current and voltage at the MPP. The programmable dc-load Chroma 63204-600 is used in constant voltage mode at 350 V, representing a stiff dc microgrid. The power analyzer Yokogawa WT1800 was used

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to record the input current, input voltage, output current, output voltage, and conversion efficiency. All the logged data are obtained in comma-separated values format, and MATLAB software is employed to analyze and visualize the data. Several scenarios are considered to evaluate the feasibility of the proposed fault diagnosis and detection system for FT ZR-SRC.

A. Fault Diagnosis and Fault Detection

1. SCF at Primary-Side MOSFETs

Different fault locations are applied to test the proposed fault diagnosis of the IB MOSFETs on the primary side. The converter is initially running in the full-bridge boost mode at 65 W. Then, an SCF of switch S_1 is introduced using an external circuitry. Fig. 8a shows that the PV voltage drops to zero, which triggers the converter malfunction of the proposed fault detection algorithm. After that, a special modulation from Table I is applied, and the voltage of the photovoltaic terminal recovers again very fast, in less than 10 ms, which means that the left leg is the faulty leg. The remedy action is applied by turning off the gating signal of both switches of the left leg while the second leg switches are modulated with the duty cycle equal to 0.5 using the APWM scheme. Also, the OB is reconfigured into a half-bridge rectifier. In the other case, when the ZR-SRC operates in the buck mode, the SCF is created at S_2, as shown in Fig. 8b. In both cases, the converter keeps running in the MPP after a fault occurrence and reconfiguration.

2. OCF at Secondary-Side MOSFETs

The OCF is created by using a series solid-state relay at the bottom switch Q_2 of the OB. As shown in Fig. 9a, once the OCF is created, the PV current starts to reduce, and then the OCF is detected based on the bottom switch voltage measurement overriding the trigger level in the microcontroller. The OCF is detected within 80 µs, which is considered negligible for PV power loss and has no harmful effect on the converter. To remedy the OCF, the top switch Q_1. Also, the resonant capacitor has a dc bias due to the half-bridge operation of the healthy OB MOSFETs with the FHR modulation after OCF. The primary winding voltage changes from bi- to uni-polar. The converter continues tracking the MPP of the PV post the fault remedy. In addition, the experimental results for OCF in Q_2 during the buck mode demonstrate the feasibility of the proposed fault diagnosis and detection, as shown in Fig. 9b.

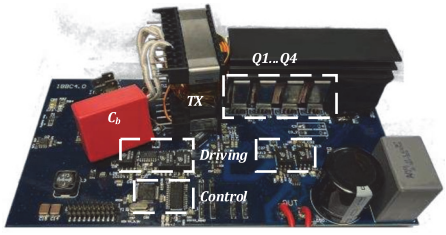

Fig. 6. Photo of the experimental setup in the laboratory.

TABLE II. PROTOTYPE PARAMETERS AND COMPONENTS

Parameter	Symbol	Value
PV input voltage range	V_{IN}	10:60 V
PV input max. current	$I_{IN,max}$	10 A
Input side capacitor	C_{IN}	150 µF
Leakage inductance	L_{lk}	100 µH
Magnetizing inductance	L_m	1 mH
Transformer turns ratio	n	12
Resonance capacitor	C_r	33 nF
Output-side capacitor	C_O	150 µF
Dc MG voltage	V_{OUT}	350 V
Switching frequency	F_{SW}	95 kHz
Components	**Symbol**	**Part Number**
Primary side switches	S_1 … S_4	FDMS86180
Secondary side switches	Q_1 … Q_4	SCT2120AF

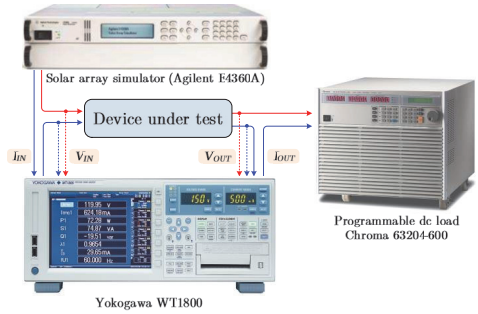

Fig. 7. Experimental setup for the data logging of the PV MPPT.

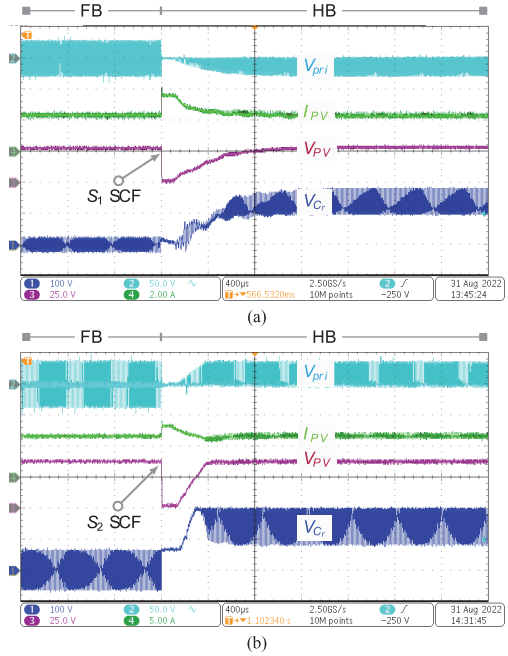

Fig. 8. SCF of input-side MOSFETs in different operating modes, locations, and operating power of the PV module: a) SCF in S_1 at the 65 W boost mode and b) SCF in S_2 at the 250 W buck mode.

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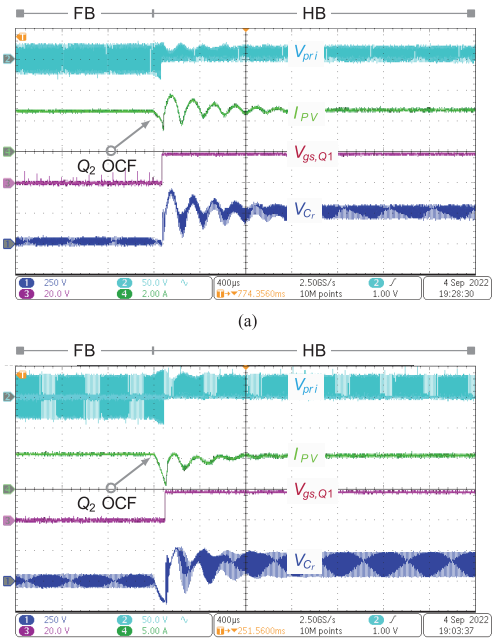

Fig. 9. OCF of the output-side MOSFETs at (a) 65 W boost mode and (b) 250 W buck mode.

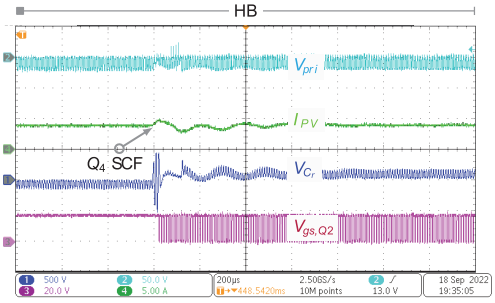

Fig. 10. SCF of the output-side MOSFETs at 75 W buck mode.

3. *Double fault cases*

In the first case, an IB MOSFET was considered damaged before the test. As a result, switch Q_4 was performing voltage boosting using the FHR modulation, while switch Q_2 was turned on continuously to reconfigure the OB in the half-bridge mode. The experimental results for the SCF in Q_4 are shown in Fig. 10. Once the SCF occurs, it is detected within 20 µs, which is less than two switching periods. In this way, the converter was protected from damage. Moreover, after the fault, the Q_2 switch is responsible for voltage boosting using the FHR modulation scheme instead of Q_4. The converter continues to perform the MPPT after the fault is remedied.

In the second case, two faults within a few seconds were considered. The experimental results validate the feasibility of remedying two faults occurring within a few seconds in Fig. 11. After both IB and OB faults, the ZR-SRC continues operating.

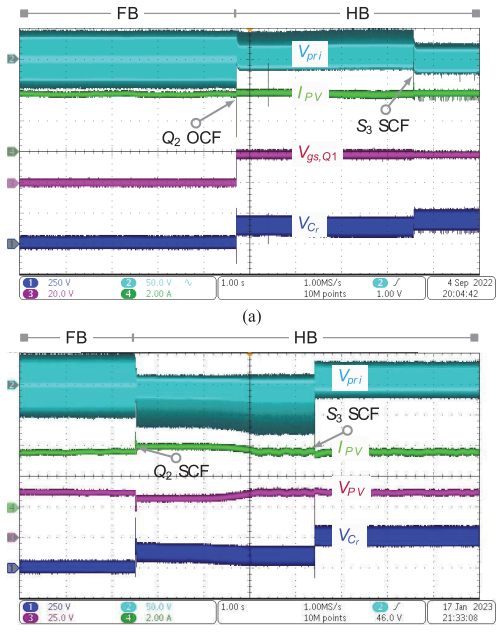

Fig. 11. Double fault in ZR-SRC with (a) OCF of Q_2 and then SCF of S_3 and (b) SCF of Q_2 and then SCF of S_3.

B. *Efficiency Evaluation Pre- and Post-Fault*

First, the converter efficiency was measured and visualized with contour plots in Fig. 12. The proposed converter maintains the post-fault efficiency close to the pre-fault levels in the main target range for unshaded PV modules, i.e., 25 V to 35 V.

Fig. 13 demonstrates energy harvested by the proposed FT converter during a day with and without a fault, with the PV module parameters given in Table III at the standard test conditions. Previous research showed that the given converter could provide the same total yearly damage to the components and avoid catastrophic failures due to overheating if its input power is clipped at the level of 200 W [33]. Hence, this value was used in the PV power clipping algorithm.

The total energy that a 60-cell Si PV module would provide at the considered environmental condition with 100% MPPT efficiency is 1355 Wh. The considered conditions correspond to a sunny day with a peak solar irradiance of 800 W/m^2. Without a fault, the proposed FT converter harvests the total energy of 1350 Wh from the PV module, corresponding to the MPPT efficiency of 99.7% MPPT efficiency during the day. However, with an SCF in the IB MOSFETs, the converter clips its input power at 200 W. Therefore, the MPPT efficiency gradually reduces to 77% as the MPP power reaches 260 W at 4.5 hr. This reduces the total harvested PV energy to 1197 Wh. This converter design exhibits similar pre- and post-fault failure rates with clipping at 200 W, as demonstrated in [33]. It is estimated that the difference between PV energy delivered in normal and faulty states is about 150 Wh, which is considered the worst-case scenario when there is no cloud cover.

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TABLE III. PV MODULE PARAMETERS IN THE AGILENT SOLAR SIMULATOR

Parameter	Symbol	Value
Cell series resistance	R_s	1 mΩ
Cell shunt resistance	R_{sh}	800 Ω
Temperature coefficient	C_t	0.00557 A/°C
Ideality factor	IF	1.4 A
Module efficiency	η	18.6 %
Open-circuit voltage	V_{OC}	40.9 V
Voltage at maximum power point	V_{MPP}	33.9 V
Short-circuit current	I_{SH}	10.77 A
Current at maximum power point	I_{MPP}	10.33 A
Maximum power	P_{MPP}	350 W

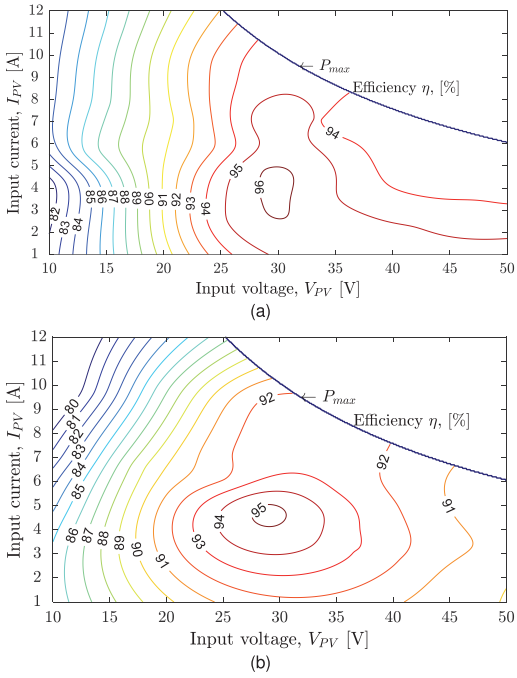

Fig. 12. Experimental efficiency maps of the ZR-SRC a) before and b) after a fault in an IB switch.

It is worth mentioning that the converter efficiency is nearly the same after a fault as before, avoiding overheating the remaining healthy components, which was considered an issue in a similar solution [17], where a significant efficiency reduction was observed after a fault. The power curtailment with converter operation above the MPP voltage was achieved.

It could be shown that the yearly energy yield would reduce by roughly 10% [33]. On the other side, FT converters significantly reduce maintenance costs, delaying the maintenance until the yearly contractual maintenance.

C. Comparison with the Existing Fault Diagnosis and Detection Techniques for Isolated FT Converters

Table IV compares the proposed comprehensive fault diagnosis and detection methods and the closest solutions. The proposed comprehensive fault diagnosis method is more effective than the closest methods for identifying faults.

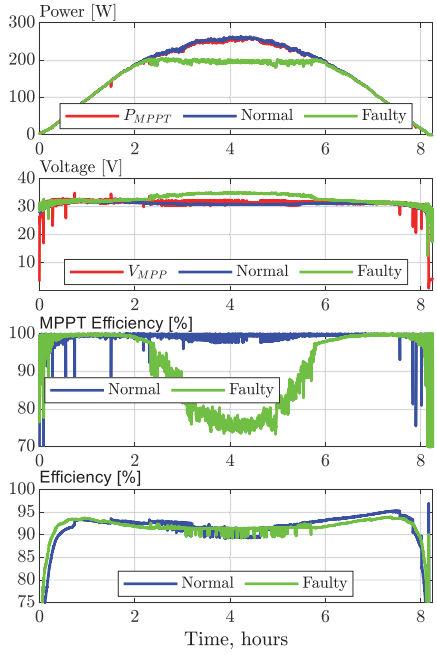

Fig. 13. Daily PV profile measurements of the ZR-SRC before and after the occurrence of a fault.

VI. CONCLUSIONS

In this paper, comprehensive diagnosis and detection methods were developed for ZR-SRC considering residential PV applications. The existing MPPT measurement signals of PV input are used to diagnose SCF in the input side of the ZR-SRC. A simple fault detection method was proposed for the output-side semiconductors. It employs a current transformer for the secondary winding current and voltage sensors of the bottom switches. Despite the low number of components, the given converter can withstand several semiconductor faults, which was not previously demonstrated for high step-up dc-dc converters. Also, it maintains voltage regulation capabilities.

The proposed converter can detect a fault accurately in 20 µs to 10 ms, depending on the fault type. No false positive detections were observed during extensive lab testing. Apart from high-speed and accurate detection, it provides on-the-fly reconfiguration with no efficiency deterioration after a fault, which distinguishes it from other similar solutions, like [17].

The random failure rate of the ZR-SRC components is kept constant before and after a fault by clipping the PV power, which does not significantly reduce the yearly energy harvest. The developed power clipping algorithm allows for the converter operation at an optimal efficiency point.

TABLE IV. COMPARISON WITH THE FAULT-DETECTION METHODS FOR ISOLATED DC-DC CONVERTERS IN THE LITERATURE WORK.

Item	[16]	[17]	Proposed
Topology	DAB	qZSN-SRC	FT ZR-SRC
Signature signals	Voltage of bottom switches in the IB and OB	Voltage of bottom IB MOSFETs beside PWM signals of the IB MOSFETs	PV voltage for IB SCF, secondary current for OB SCF, and voltage of OB MOSFETs for OB OCF
Fault type	OCF	Only SCF in the IB	SCF/OCF
Number of cascaded faults	2	1	2
Total fault types	8	4	8
Number of sensors	4	2	3

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